

Compal Confidential

DIUYA/YB/SA/SB/SD (KBL-R)

DIS M/B Schematics Document

Intel KabyLake U/KabyLake R Processor with DDR4

N16S-GTR(940) (23x23mm)
N16V-GMR1(920) (23x23mm)

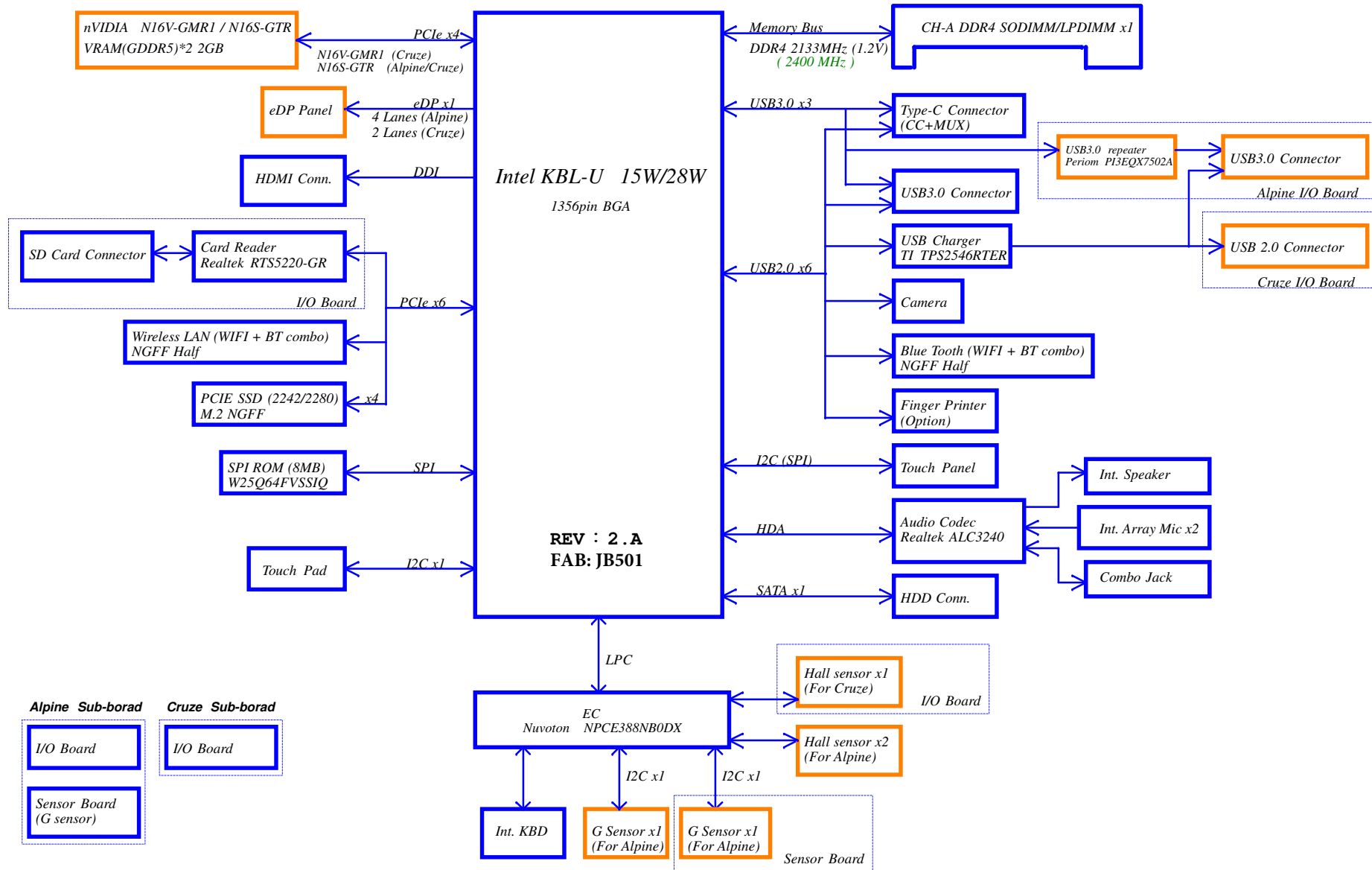
2017-06-05

LA-E541P

REV : 2.A

FAB: JB501

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Voltage Rails

power plane	B+	+5VALW	+1.2V	+5VS +3VS +1.35VS +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG
State		+3VALW		+1.8VS +0.6VS +1.0VALW
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
For DIS	DIS@
For UMA	UMA@
For Touch Panel with SPI	TS_SPI@
For Touch Panel with I2C	TS_I2C@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For Samsung VRAM	S2G@
For Micron VRAM	M2G@
For Hynix VRAM	H2G@
For UHD Panel	UHD@
For Finger Printer	FP@
For SSD	SSD@
For EMI	EMI@
For ESD	ESD@
For RF	RF@
No EMI	@EMI@
No ESD	@ESD@
No RF	@RF@
Connector	ME@
For VARM X76	X76@
For Test Point	TP@
For Debug	@DCI@
For S series only	S_AL@
For S IMR series only	S_IMR@
For YOGA series only	YOGA@
For CPU Type	17_7500U_R1@ 15_7200U_R1@ i3_7100U_R1@ 17_7500U_R3@ 15_7200U_R3@ i3_7100U_R3@ pt_4415U_R1@ pt_4415U_R3@ i3_6006U_R3@

Item	BOM Structure
For KBL U22 CPU	U22@
For KBL U42 CPU	U42@
For GPU Type	N16S_R1@ N16S_R3@ N16V_R1@ N16V_R3@
For EMI	U22_EMI@ U42_EMI@
For Thermal sensor	EX_THM@
For ESD	FP_ESD@

USB 2.0 Port Table

Port	External USB Port
1	USB3 Type-C Port
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	USB3 Type-C Port
5	Camera
6	Finger Printer (Option)
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	External USB Port
1	USB3 Type-C (MUX)
2	USB2/3 Port (MB)
3	USB2/3 Port (IO/B)
4	
5	
6	

SATA Port Table

Port	External SATA Port
0	HDD
1	

PCIe Port Table

Lane	Port	External PCIe Port
1		
2		
3	1	GPU
4		
5		Card Reader
6		NGFF WLAN+BT
7		
8		
9		
10		
11	3	SSD
12		

EC SM Bus1 address EC SM Bus2 address EC SM Bus4 address

Device	Address	Device	Address	Device	Address
Smart Battery	0001 011x 16h	NC77718W	1001 100x 98h	BMA250E	0001 100x 18h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU			TP	PCH	G-SENSOR
SMB_EC_CK1	NECP388	X	V	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW	+19V_VIN									
SMB_EC_CK2	NECP388	X	X	X	X	X	X	X	X	X	X	X	X
SMB_EC_DA2	+3VGS				+3VS						+3VS		
SMB_EC_CK4	NECP388	X	X	X	X	X	X	X	X	X	X	X	X
SMB_EC_DA4	+3VALW												+3VS
PCH_SMBCLK	PCH	X	X	X	X	X	X	X	X	X	X	X	X
PCH_SMBDATA	+3VALW										+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW										+3VS		
SML1CLK	PCH	X	X	X	X	X	X	X	X	X	X	X	X
SML1DATA	+3VALW										+3VS		

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

X4E

Yoga Series ZZZ4 X4E_YA@ ZZZ3 X4E_YA_FP@ ZZZ5 X4E_YB@ ZZZ6 X4E_YB_FP@ X4E Y Series X4EASR3BLA1 X4E Y Series FP SKU X4EASR3BLA2 X4E Y Series UHD SKU X4EASR3BLA2 X4E Y Series UHD+FP SKU X4EASR3BLA1	S Series ZZZ9 X4E_S@ ZZZ7 X4E_S_FP@ X4E S Series X4EASR3BLA1 X4E S Series FP SKU X4EASR3BLA2	HDMI Logo ZZZ 45@ HDMI Logo R0000003HM
Yoga Series (U42) ZZZ X4E_U42_YA@ ZZZ X4E_U42_YA_FP@ ZZZ1 X4E_U42_YB@ ZZZ2 X4E_U42_YB_FP@ X4E Y Series X4EASR3BLA2 X4E Y Series FP SKU X4EASR3BLA1 X4E Y Series UHD SKU X4EASR3BLA2 X4E Y Series UHD+FP SKU X4EASR3BLA1	S Series (U42) ZZZ X4E_U42_S@ ZZZ X4E_U42_S_FP@ X4E S Series X4EASR3BLA1 X4E S Series FP SKU X4EASR3BLA2	PCB part ZZZ YOGA@ PCB Y Series DA000195A ZZZ S_AL@ PCB S Series DA000195A ZZZ S_IMR@ PCB S Series DA000195A
GDDR5 VRAM * 2 X7671138L03 U6 S2G@ U7 S2G@ K4G80325FB-HC03 SA000094R20 RV65 SDQ34499180 1.99K_0402_1% S2G@	X7671138L02 U6 M2G@ U7 M2G@ MT51J256M32HF SA000096R20 RV65 SDQ34100280 10K_0402_1% M2G@	X7671138L01 U6 H2G@ U7 H2G@ H5GC8H24MJR-T2C SA000092G10 RV65 SDQ34301280 30.1K_0402_1% H2G@

GPU part

U1 N16S_R1@ N16S-GTR-S-A2 BGA 595P SA000097P00	U1 N16V_R1@ N16V-GMR1-S-A2 BGA 595P SA000097T00
U1 N16S_R3@ N16S-GTR-S-A2 BGA 595P SA000097P00	U1 N16V_R3@ N16V-GMR1-S-A2 BGA 595P SA000097T00

CPU part

KBL U22 (= U22@) UC1 i3_7100U_R1@ UC1 i5_7200U_R1@ UC1 i7_7500U_R1@ UC1 pt_4415U_R1@ QLYKH H0 2.4G SA0000A3B80 QLYYH H0 2.5G SA0000A3780 QLYYH H0 2.7G SA0000A3480 QLYYH H0 2.9G SA0000ADV00	SKL U22 (= U22@) UC1 i3_6006U_R3@ SR2JG R1 i3-6006U 2.0G C381 SA0000ACN10	KBL U42 (= U42@) UC1 i5_QNBF_R1@ UC1 i7_QNBF_R1@ QNEFY Y0 1.6G FCBGA SA0000AWB00 QNEFY Y0 1.6G FCBGA SA0000AWC00
UC1 i3_7100U_R3@ UC1 i5_7200U_R3@ UC1 i7_7500U_R3@ UC1 pt_4415U_R3@ SR343 H0 2.4G SA0000A3B80 SR342 H0 2.5G SA0000A3780 SR341 H0 2.7G SA0000A3480 SR348 H0 2.9G SA0000ADV20		UC1 i5_QNBF_R3@ UC1 i7_QNBF_R3@ QNEFY Y0 1.6G FCBGA SA0000AWB50 QNEFY Y0 1.6G FCBGA SA0000AWC50

-PowerMap_KBL_DDR4_Volume_NON CS]

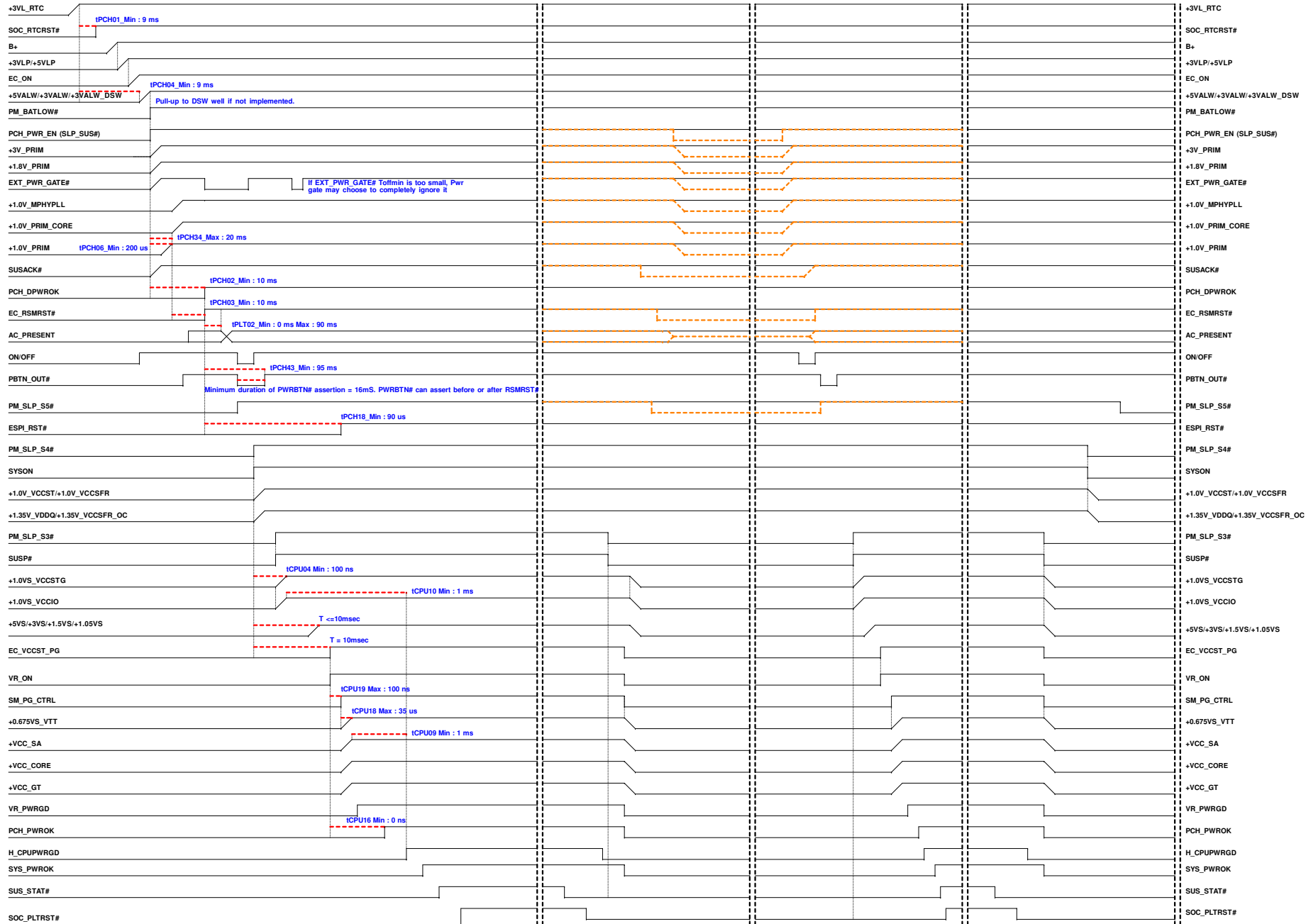


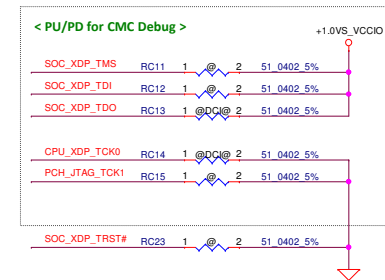
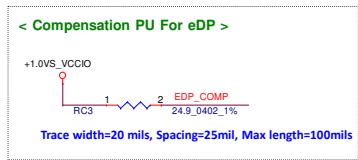
G3->S0

S0->S3/DS3

S0/DS3->S0

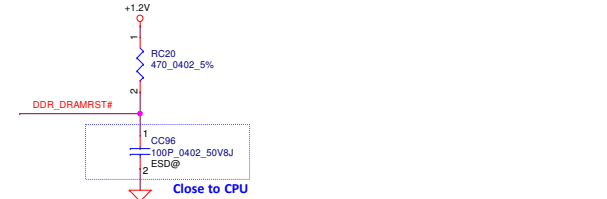
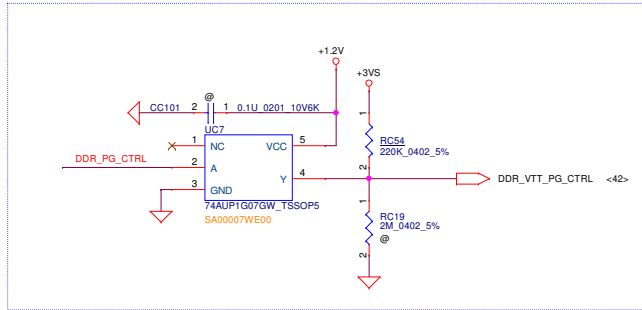
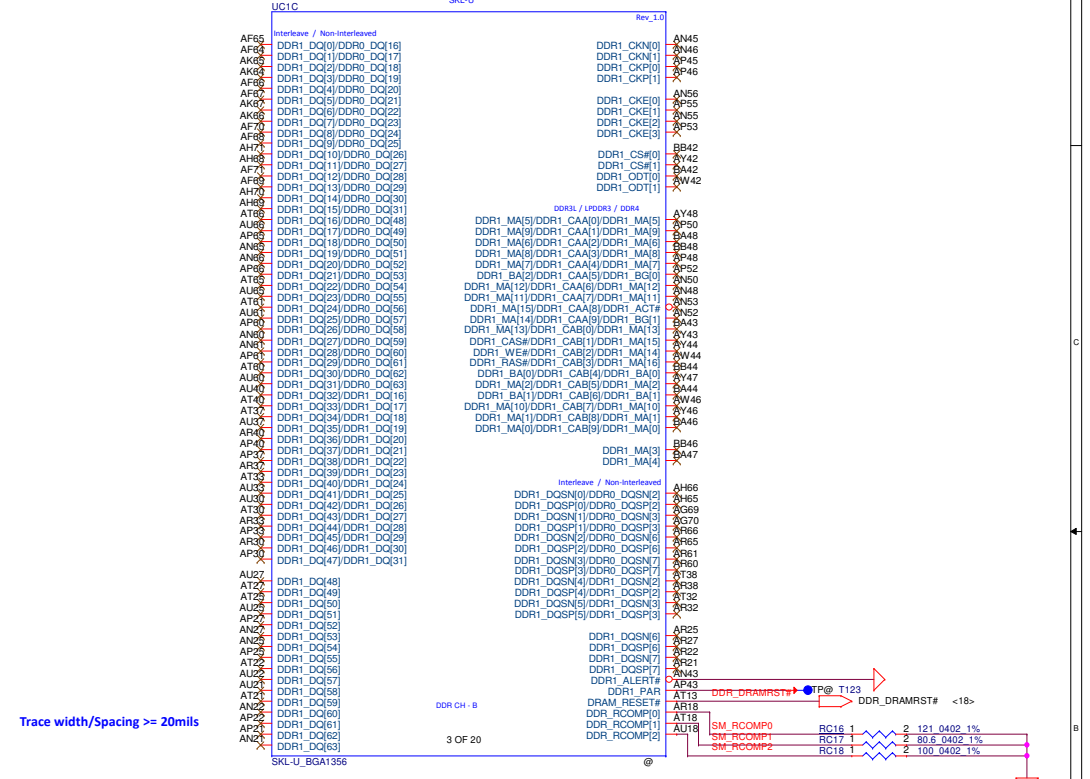
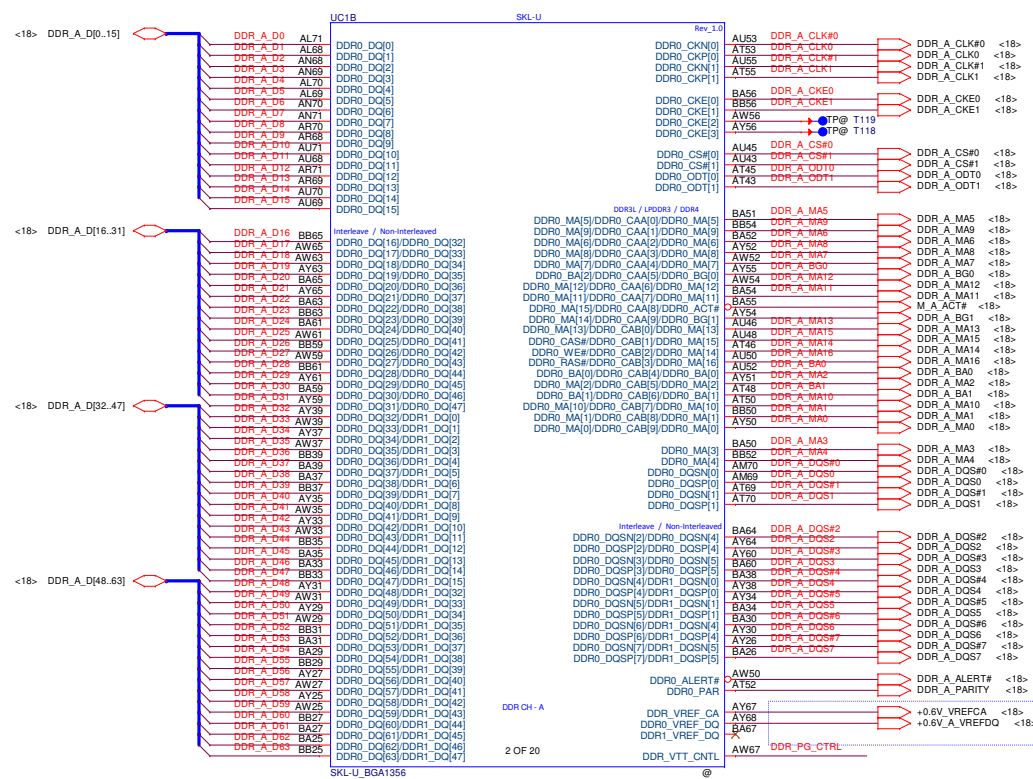
S0->S5



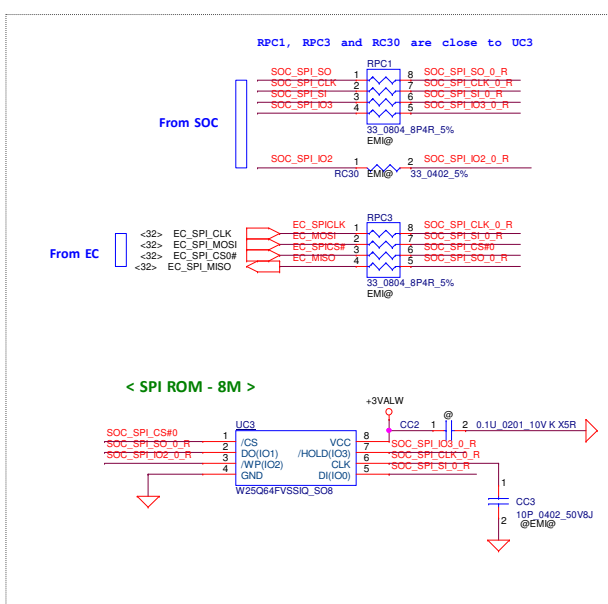
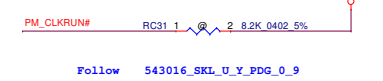
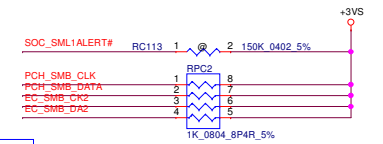
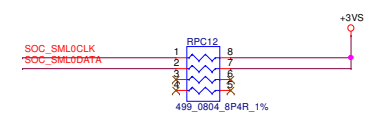
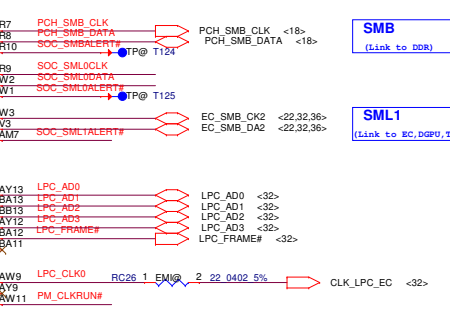
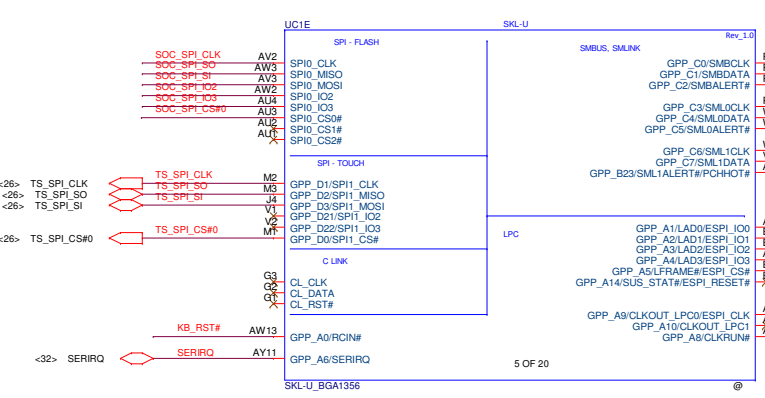
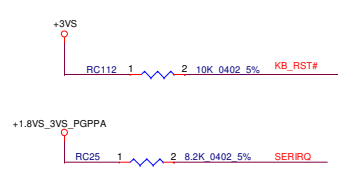
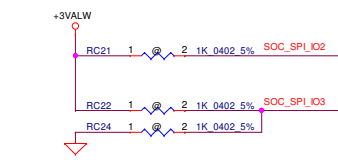


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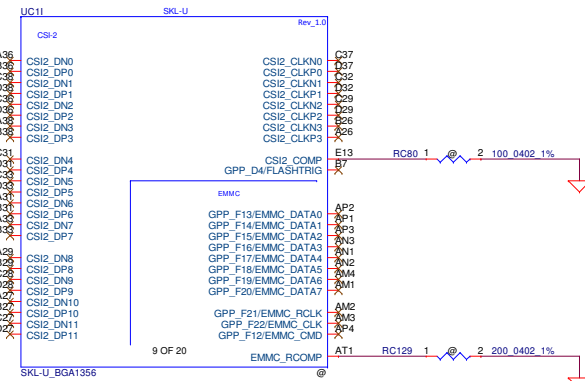
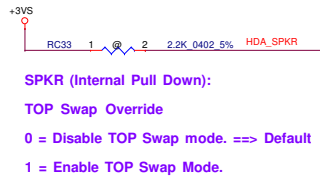
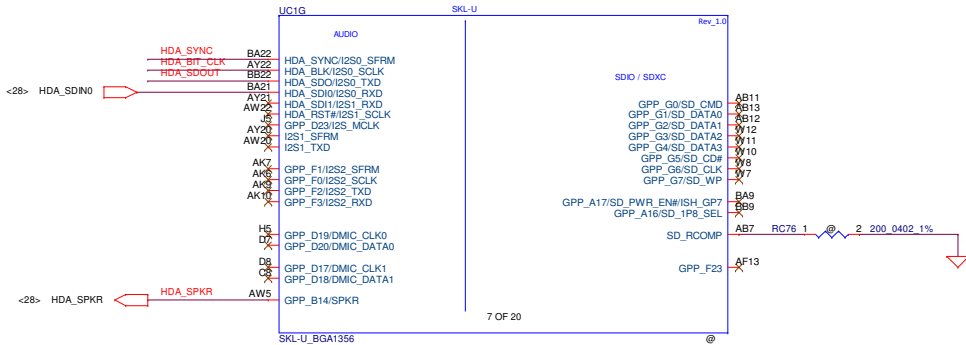
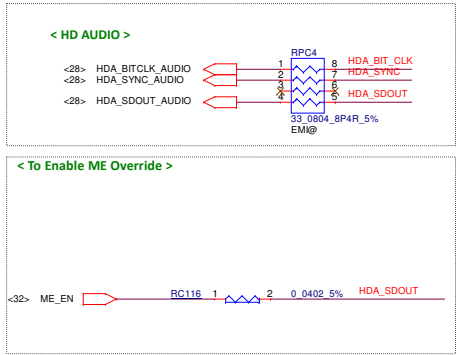
Interleaved Memory



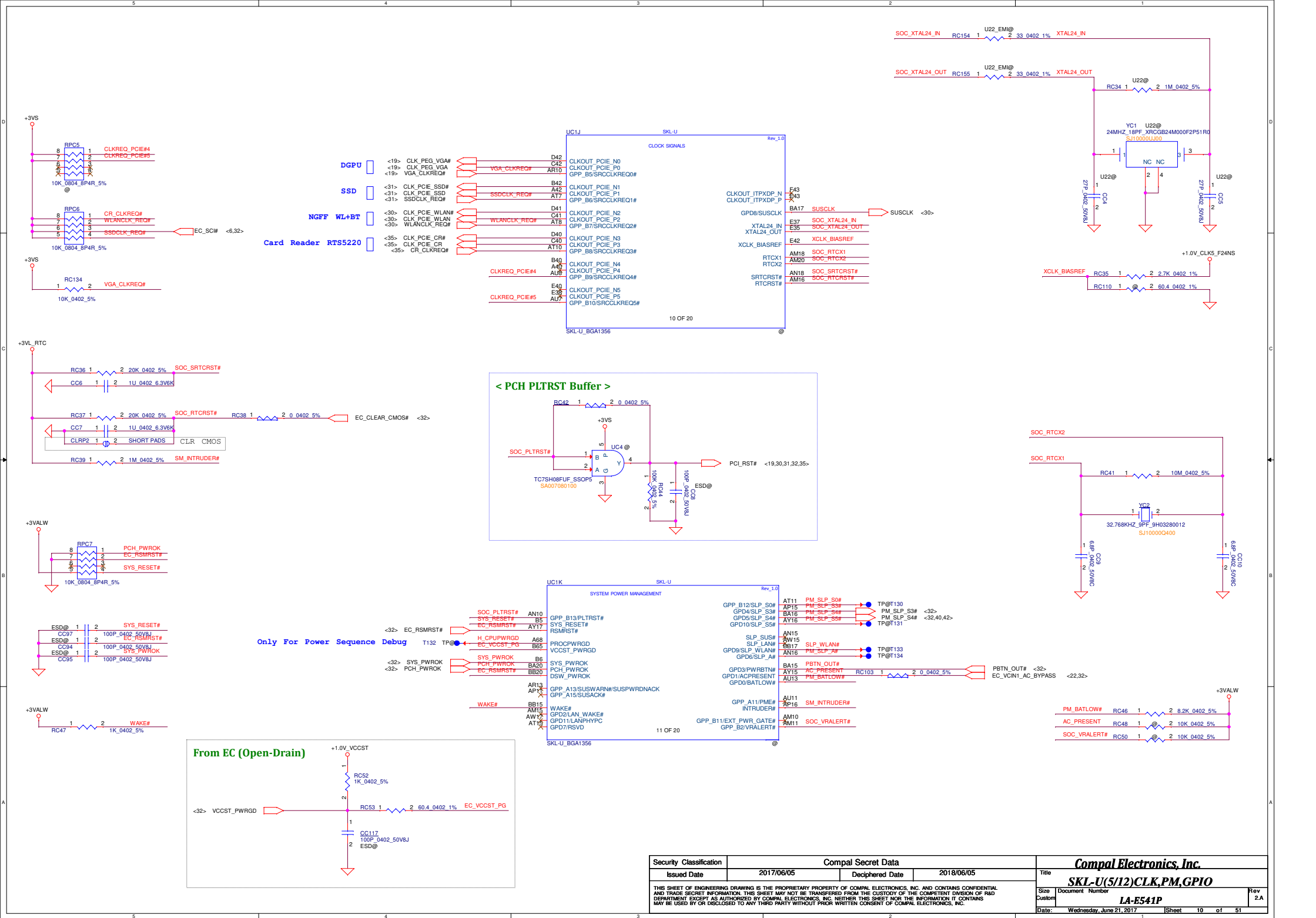
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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

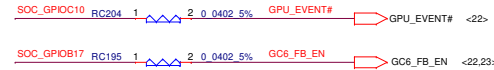
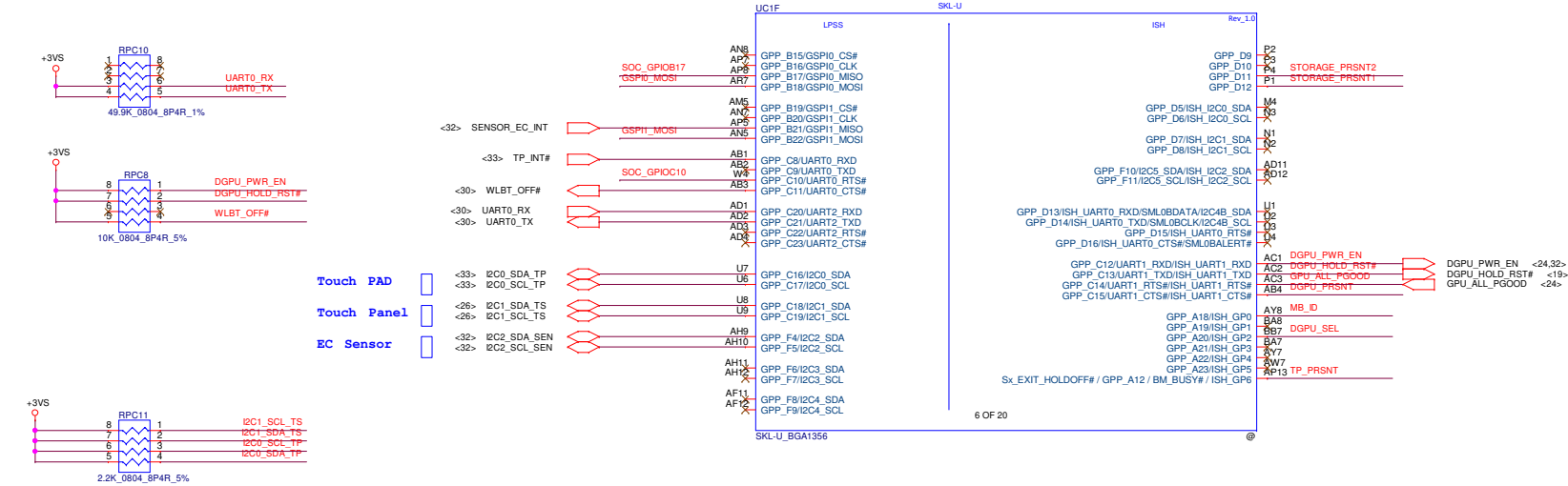
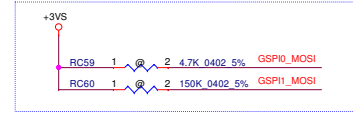
1 = Enable No Reboot Mode. (PCH will disable the TCO
Timer system reboot feature). This function is used
when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

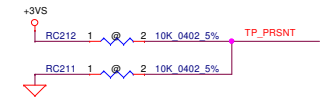
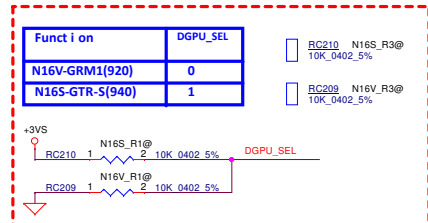
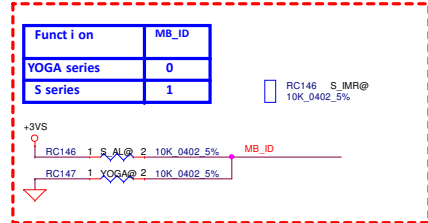
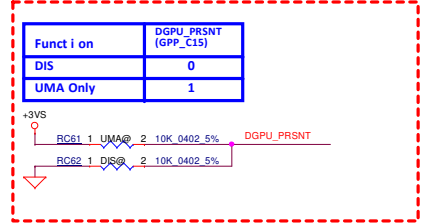
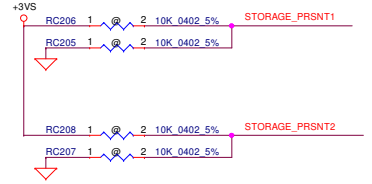
Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode



TO DGPU



dGPU

Card Reader

NGFF WLAN+BT

HDD

SSD

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<19> PCIE_PTX_C_DRX_N1
<19> PCIE_PTX_C_DRX_P1

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<19> PCIE_PTX_C_DRX_N2
<19> PCIE_PTX_C_DRX_P2

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<19> PCIE_PTX_C_DRX_P3

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<31> PCIE_PTX_C_DRX_P12

CC11 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N1
CC14 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P1

CC15 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N2
CC16 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P2

CC12 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N3
CC13 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P3

CC17 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N4
CC18 DIS@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P4

CC19 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_N5
CC20 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_P5

CC102 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_N6
CC103 1 2 0.1U 0201 10V K XSR PCIE_PTX_DRX_P6

CC110 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N9
CC109 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P9

CC114 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N10
CC113 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P10

RC71 1 2 100 0402 1% PCIE_ROMPN
PCIE_ROMMP

T147 TP@ XDP_PRODM
T148 TP@ XDP_PREDM

CC116 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N11
CC115 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P11

CC112 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_N12
CC111 SSD@ 1 2 0.22U 0402 6.3V6K PCIE_PTX_DRX_P12

UC1H @

SKL-U

Rev_1.0

PCIE / USB3 / SATA

SSIC / USB3

USB2

SKL-U_BGA1356

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USB3_1_RXN
USB3_1_RXP
USB3_1_TXN
USB3_1_TXP

USB3_2_RXN / SSIC_RXN
USB3_2_RXP / SSIC_RXP
USB3_2_TXN / SSIC_TXN
USB3_2_TXP / SSIC_TXP

USB3_3_RXN
USB3_3_RXP
USB3_3_TXN
USB3_3_TXP

USB3_4_RXN
USB3_4_RXP
USB3_4_TXN
USB3_4_TXP

USB2N_1
USB2P_1

USB2N_2
USB2P_2

USB2N_3
USB2P_3

USB2N_4
USB2P_4

USB2N_5
USB2P_5

USB2N_6
USB2P_6

USB2N_7
USB2P_7

USB2N_8
USB2P_8

USB2N_9
USB2P_9

USB2N_10
USB2P_10

USB2_COMP
USB2_ID
USB2_VBUSSENSE

GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#

GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2

GPP_E0/SATAXP/PCIE0/SATAP0
GPP_E1/SATAXP/PCIE1/SATAP1
GPP_E2/SATAXP/PCIE2/SATAP2

GPP_E8/SATALED#

H8
G6
C13
D13

J6
H6
B13
A13

J10
B15
A15

E10
C10
C15
A15

AB9
AB10

AD6
AD7

AH3
AH5

AD9
AD10

AJ1
AJ2

AF6
AF7

AH1
AH2

AF8
AF9

AG1
AG2

AH7
AH8

AB6
AG3
AG4

A9
C9
D9
B9

J1
J2
J3
N1

H2
H3
H4
H1

USB3_RX1_N
USB3_RX1_P
USB3_TX1_N
USB3_TX1_P

USB3_RX2_N
USB3_RX2_P
USB3_TX2_N
USB3_TX2_P

USB3_RX3_N
USB3_RX3_P
USB3_TX3_N
USB3_TX3_P

USB20_N1
USB20_P1

USB20_N2
USB20_P2

USB20_N3
USB20_P3

USB20_N5
USB20_P5

USB20_N6
USB20_P6

USB20_N7
USB20_P7

USB_OC0#
USB_OC1#
USB_OC2#

WL_OFF#

RC70 1 2 113 0402 1%
RC104 1 2 1K 0402 5%
RC105 1 2 1K 0402 5%

RC139 1 2 10K 0402 5%

USB3 Type-C (MUX)

USB2/3 Port (MB)

USB2/3 Port (IO/B)

USB3 Type-C Port

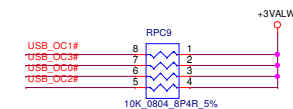
USB2/3 Port (MB)

USB2/3 Port (IO/B)

Camera

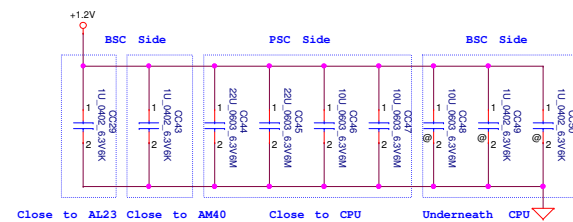
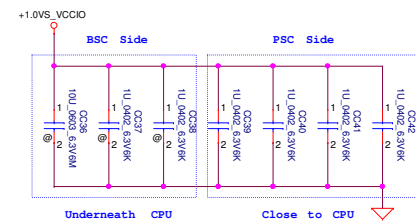
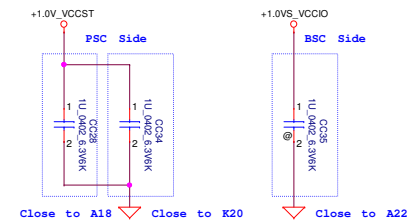
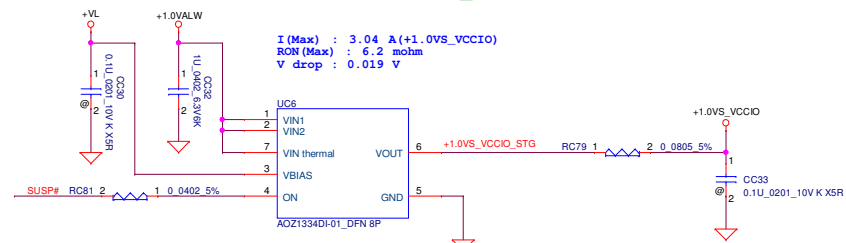
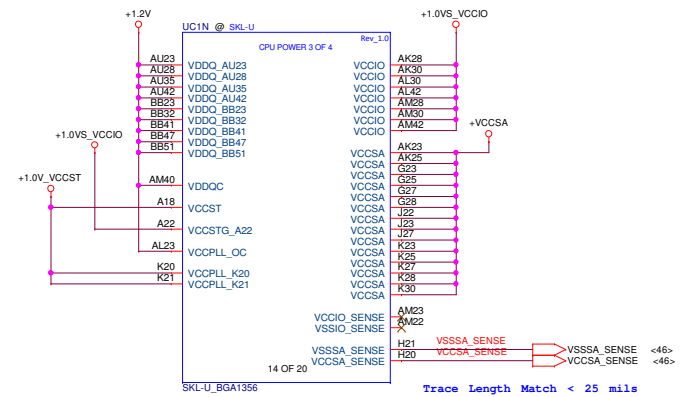
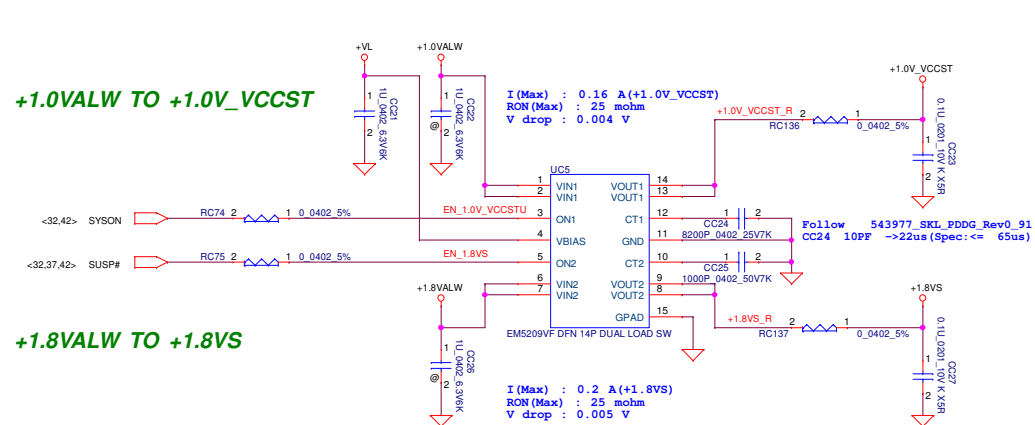
Finger Printer

NGFF WLAN+BT

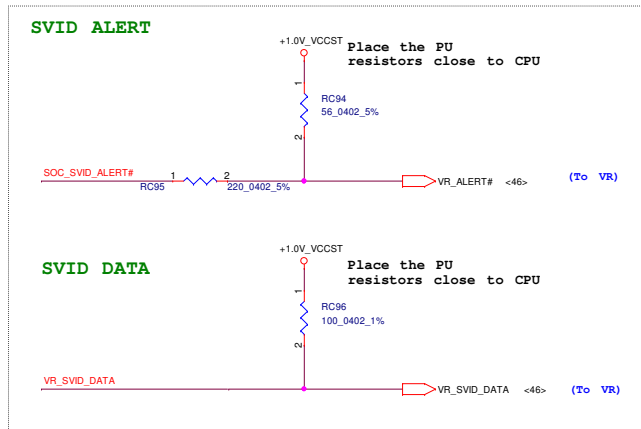
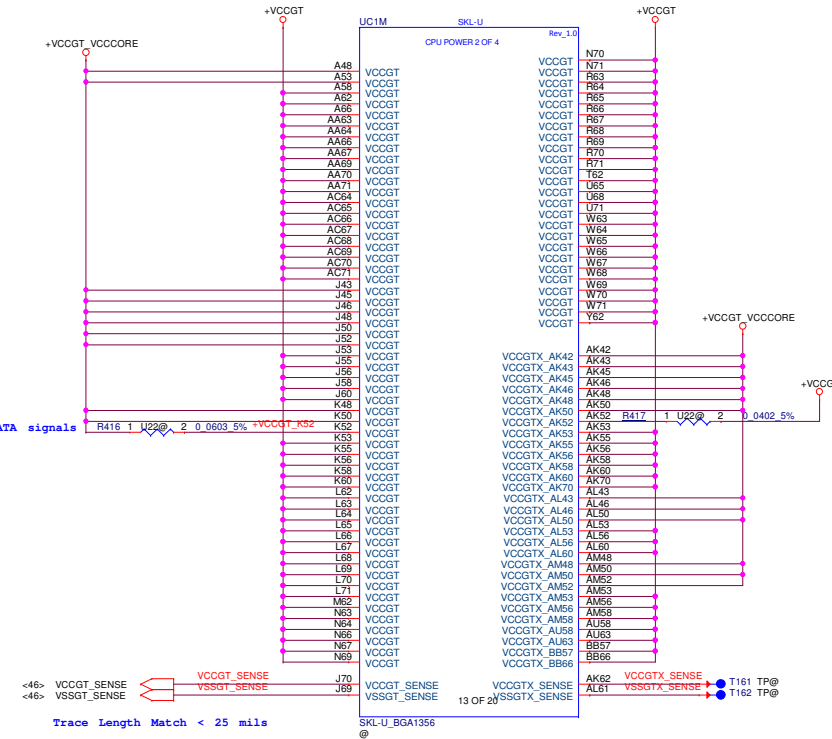
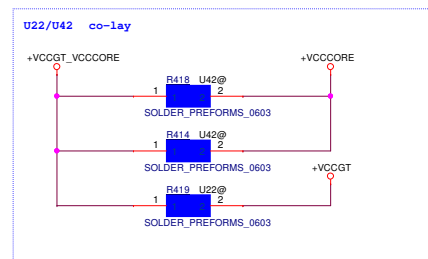
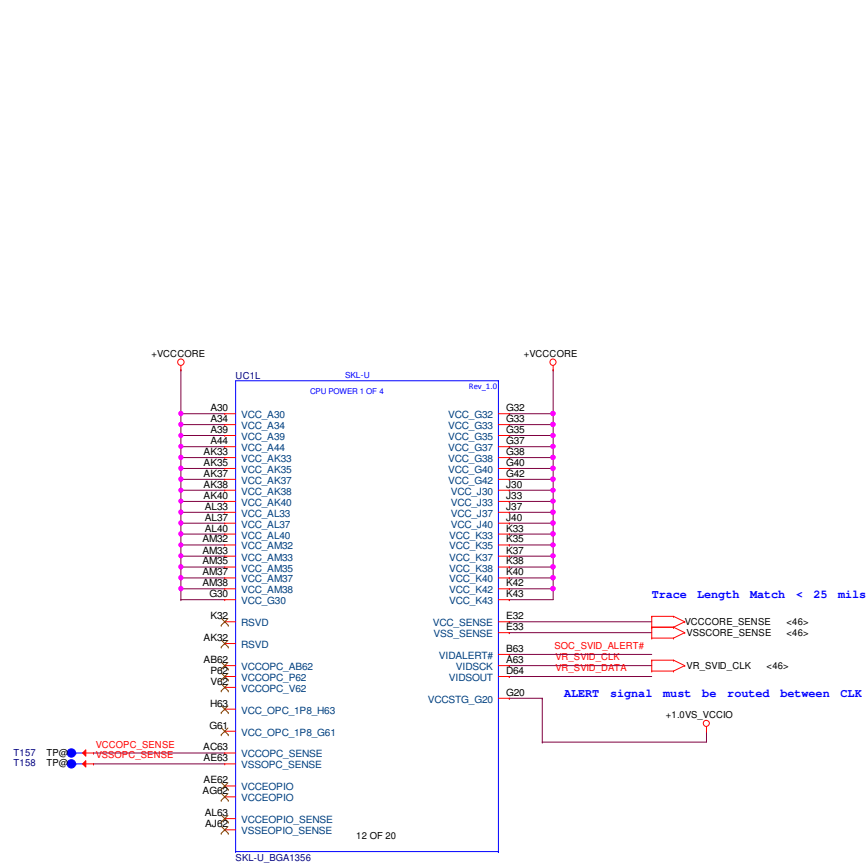


When PCIE8/SATA1A is used as SATA Port 1 (ODD), then
PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

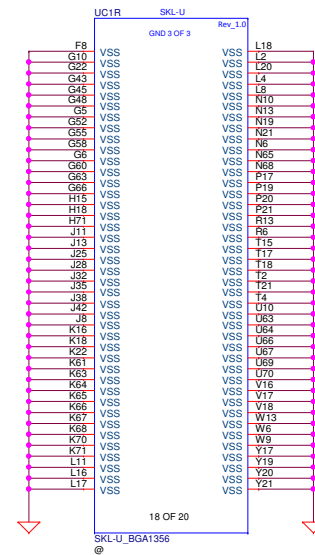
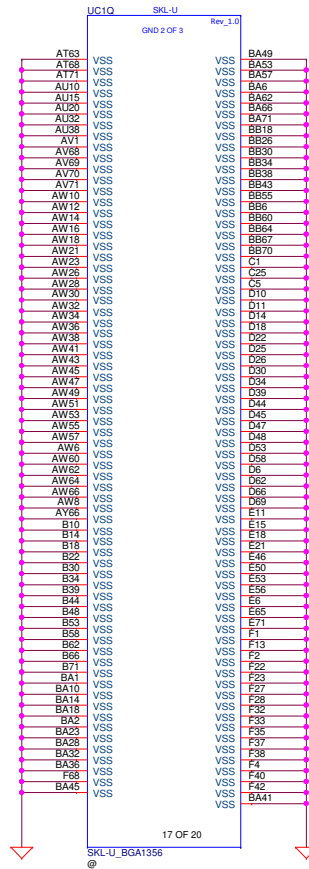
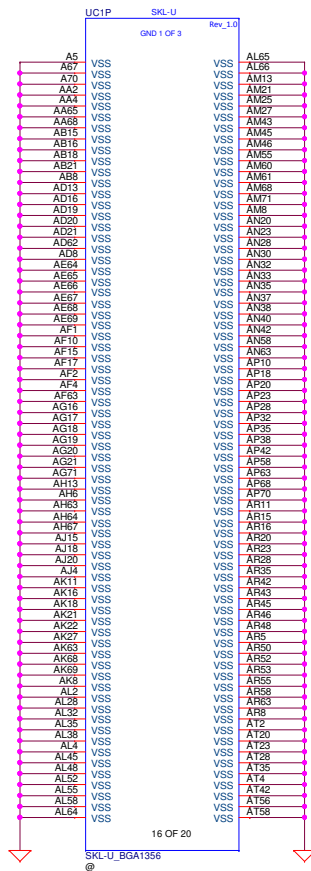
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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	
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				Date	Wednesday, June 21, 2017
				Sheet	12 of 51
				Rev	2A



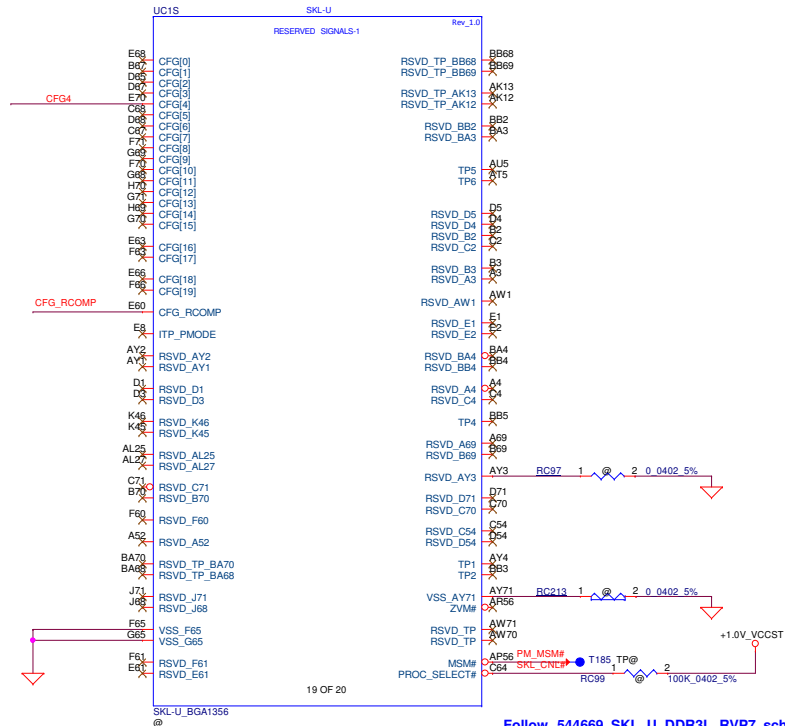
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				Custom	LA-E541P	2A
				Date:	Wednesday, June 21, 2017	Sheet 13 of 51



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								Document Number			
								Rev			
								Date			
								Wednesday, June 21, 2017			
								Sheet 15 of 51			



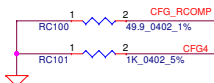
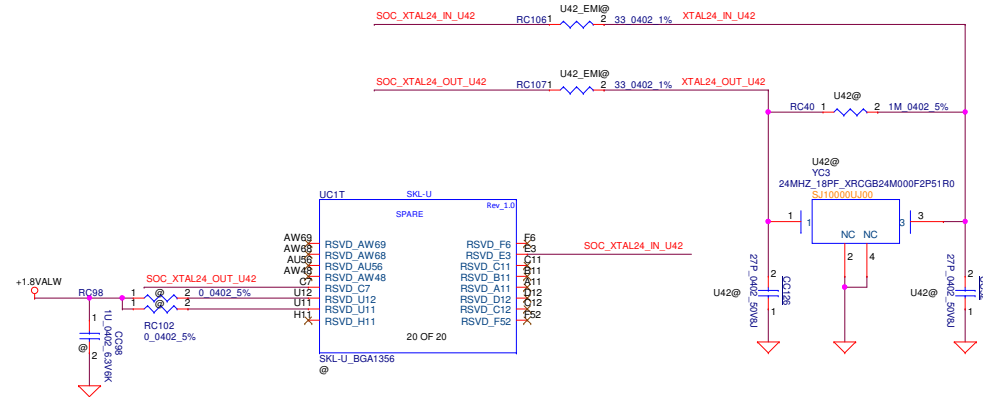
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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	
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				Size	Rev
				Custom	2A
				LA-E541P	
Date: Wednesday, June 21, 2017				Sheet	16 of 51



Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

Stuff 100k(RC99) for CannonLake-U

Un-stuff 100k(RC99) for SkyLake-U



Display Port Presence Strap

CFG4

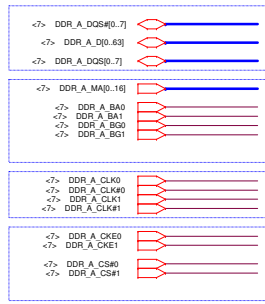
1 : Disabled;
No Physical Display Port attached to Embedded Display Port

0 : Enabled;
An external Display Port device is connected to the Embedded Display Port

Security Classification		Compal Secret Data		Title	
Issued Date	2017/06/05	Deciphered Date	2018/06/05	SKL-U(12/12)CFG,RSVD	
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				LA-E541P	
				Date:	Wednesday, June 21, 2017
				Sheet	17 of 51

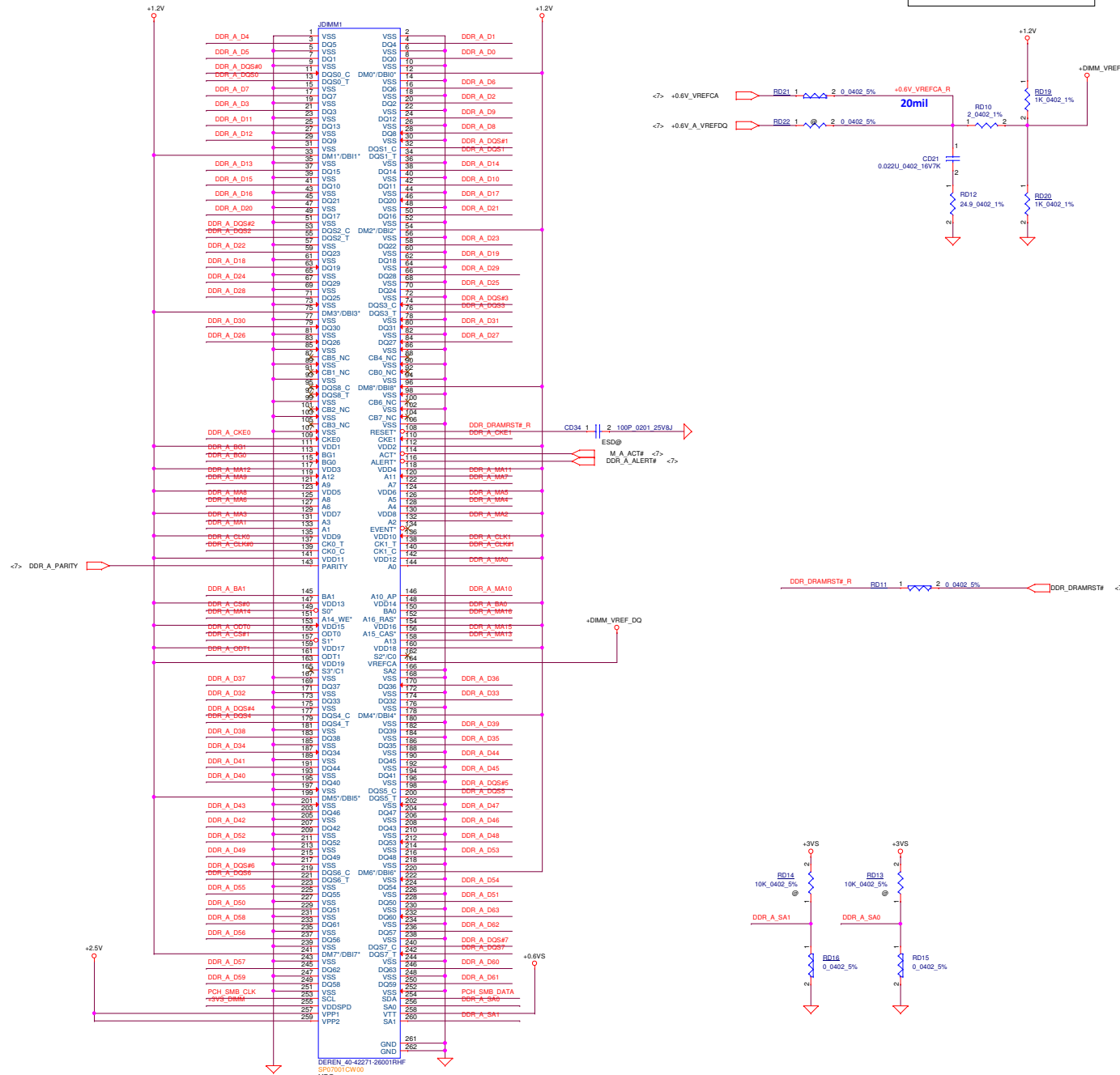
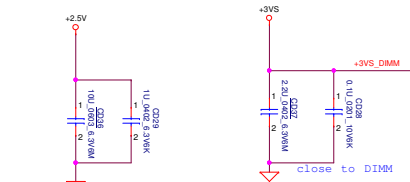
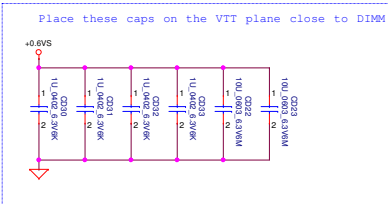
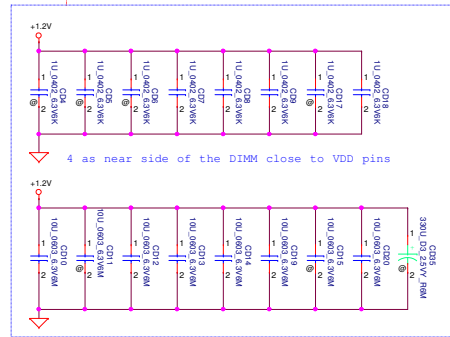
Interleaved Memory

Reverse Type
2-3A to 1 DIMMs/channel



Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

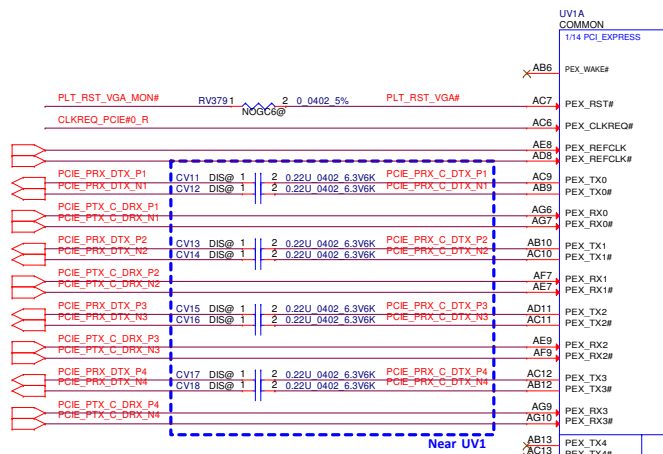


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Issued Date	2017/06/05	Deciphered Date	2018/06/05	DDR4 DIMM	
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Date: Wednesday, June 21, 2017				Sheet	18 of 51

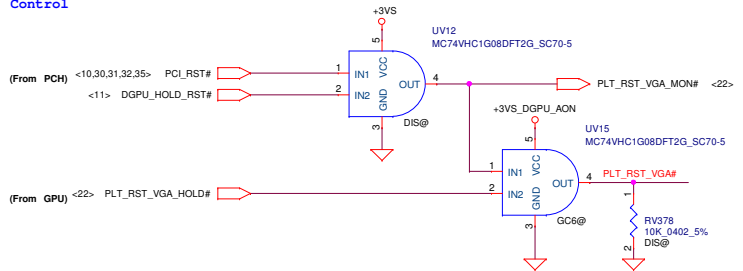
PCIE CLK

PCIE X4 Bus

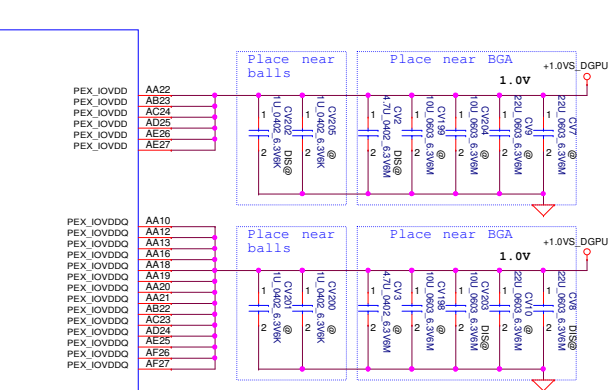
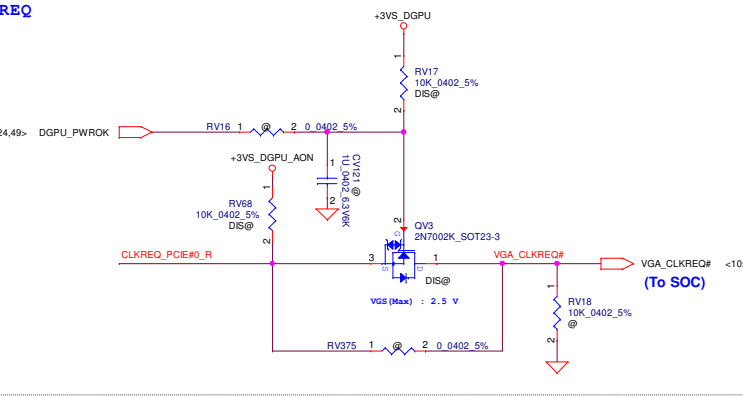
- <10> CLK_PEG_VGA
- <10> CLK_PEG_VGA#
- <12> PCIE_PRX_DTX_P1
- <12> PCIE_PRX_DTX_N1
- <12> PCIE_PTX_C_DRX_P1
- <12> PCIE_PTX_C_DRX_N1
- <12> PCIE_PRX_DTX_P2
- <12> PCIE_PRX_DTX_N2
- <12> PCIE_PTX_C_DRX_P2
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- <12> PCIE_PTX_C_DRX_P3
- <12> PCIE_PTX_C_DRX_N3
- <12> PCIE_PRX_DTX_P4
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- <12> PCIE_PTX_C_DRX_P4
- <12> PCIE_PTX_C_DRX_N4



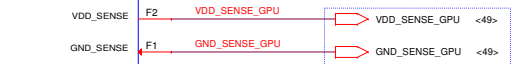
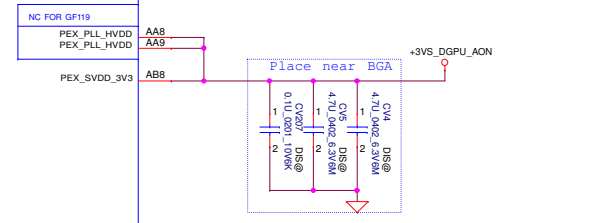
Reset Control



CLK_REQ

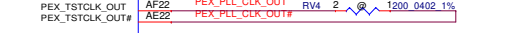


NC FOR GF119

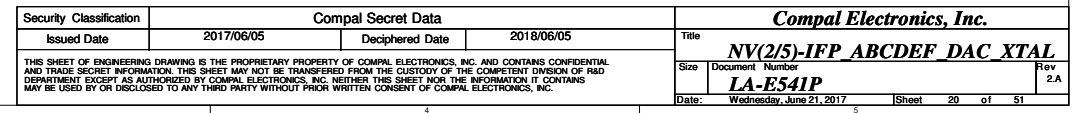
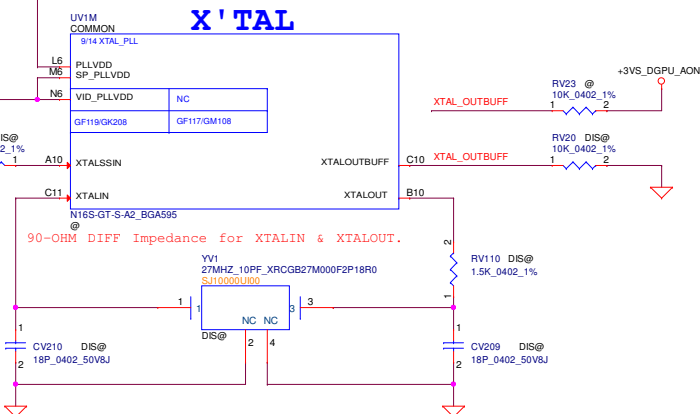


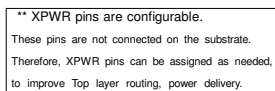
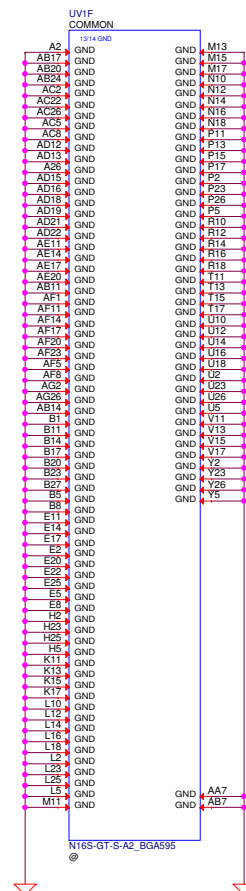
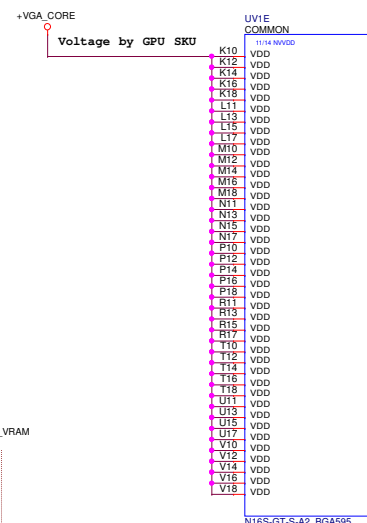
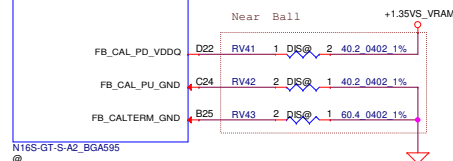
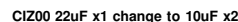
To POWER

trace width: 16mils
differential voltage sensing.
differential signal routing.

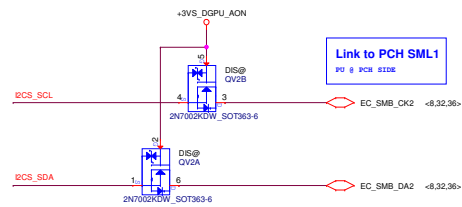
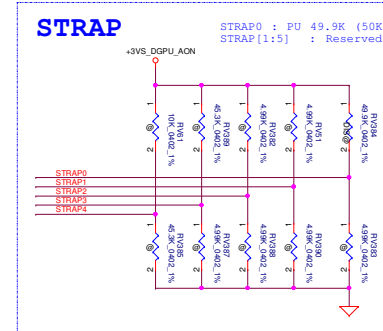
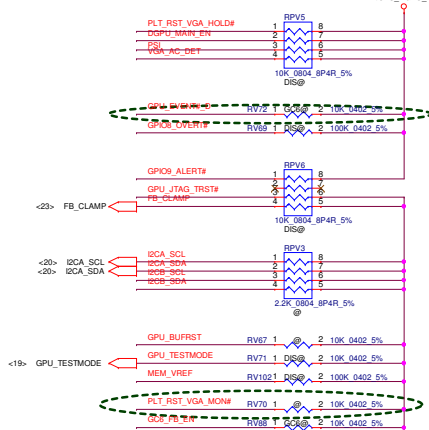


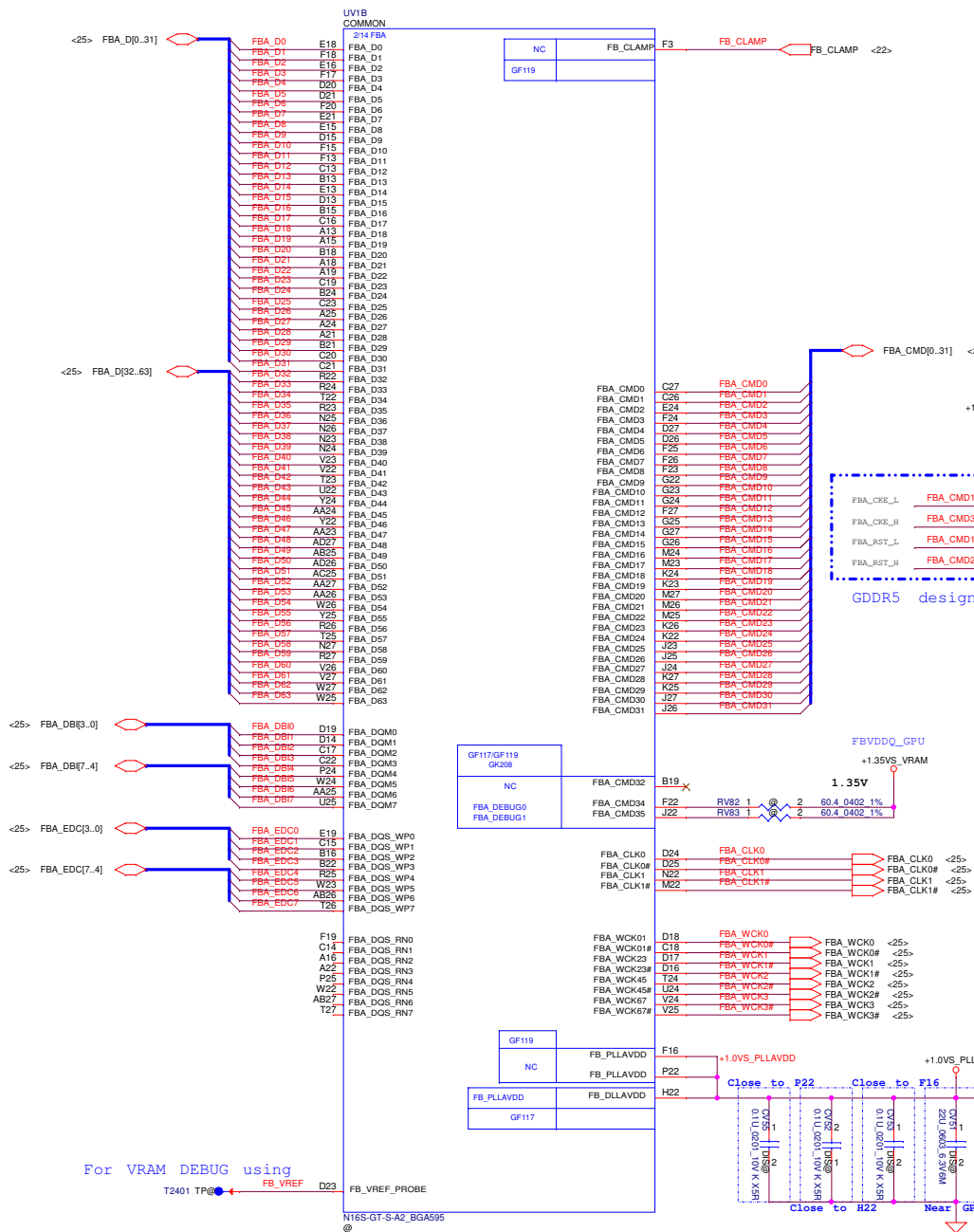
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	NV(1/5)-PCIE
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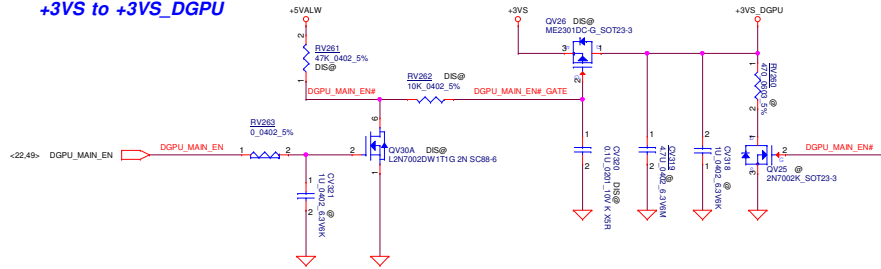


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						Document Number		Rev
						LA-E541P		2.A
Date:		Wednesday, June 21, 2017		Sheet	21	of 51		



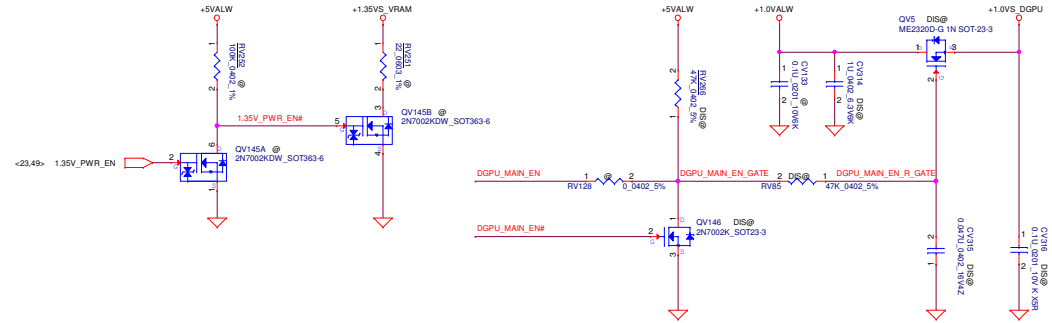


+3VS to +3VS_DGPU

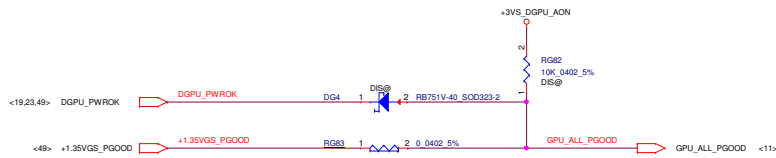
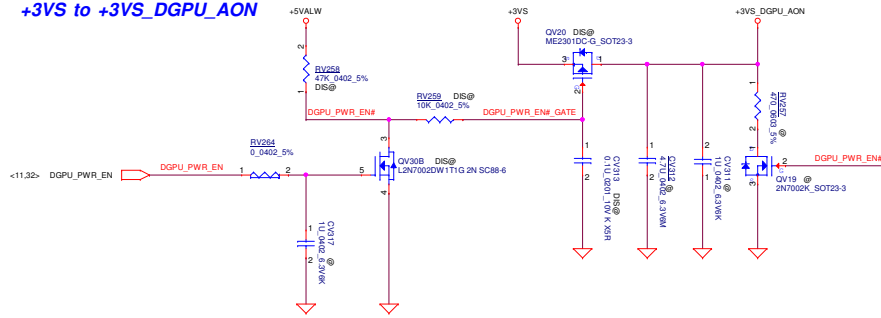


+1.0V_PRIM to +1.0VS_DGPU

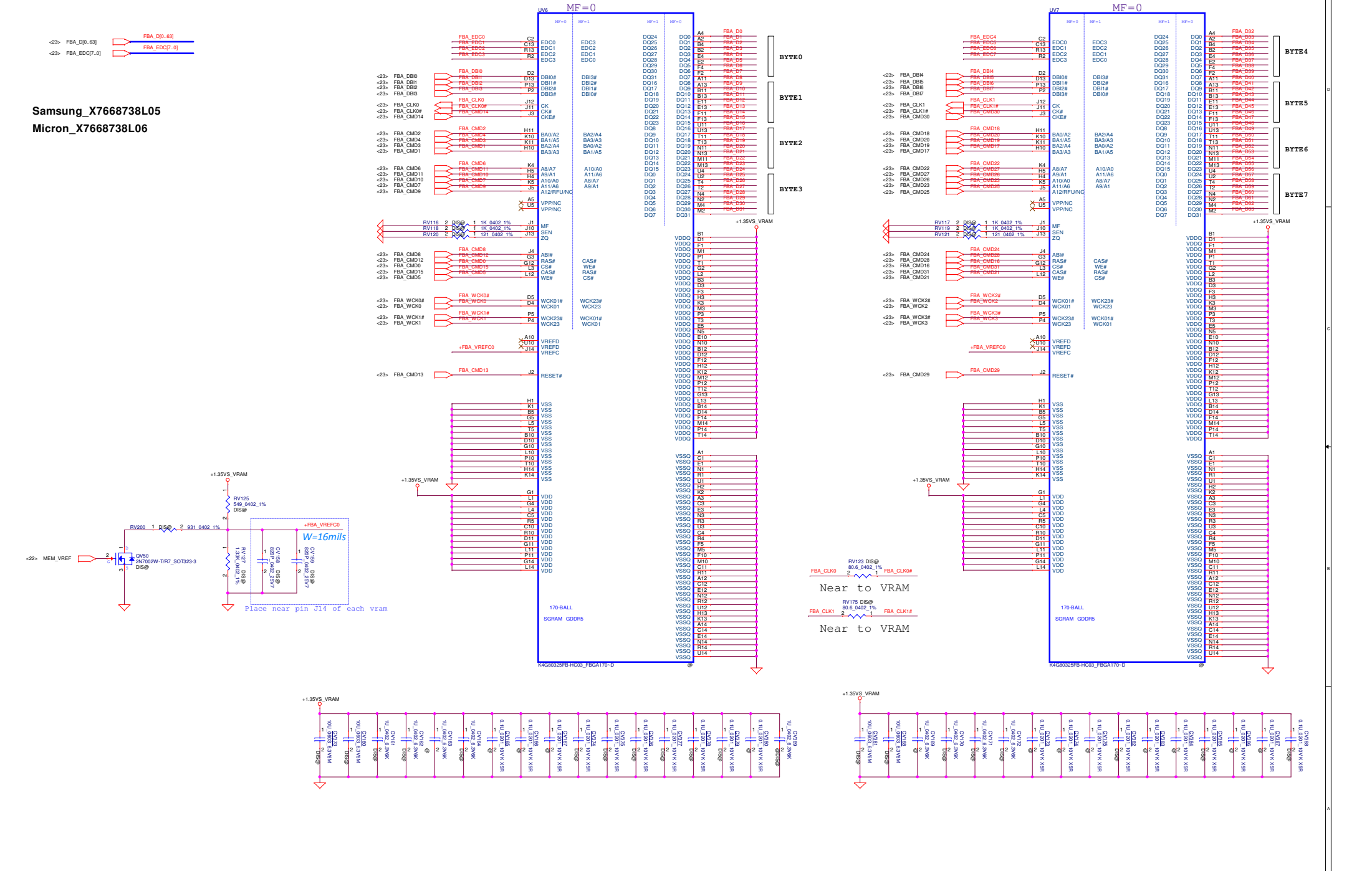
I Continuous (Max) : 0.79 A(+1.0VS_DGPU)
 RON (Max) : 22 mohm
 V drop : 0.0175 V
 Rising : ~ 208us

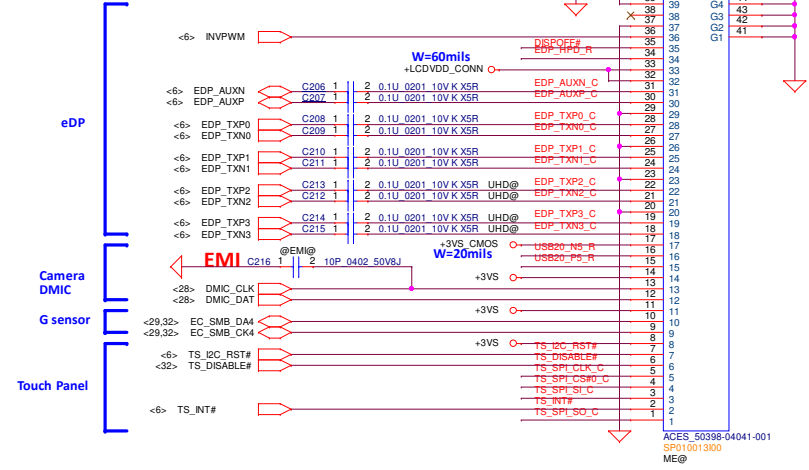
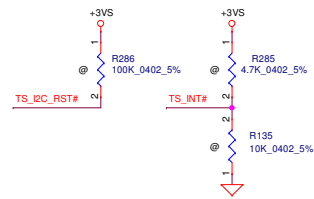
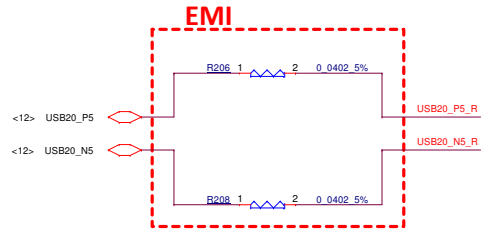
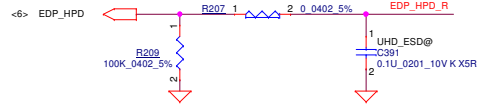
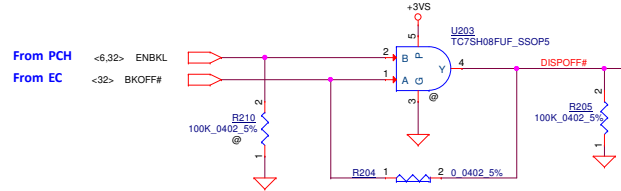
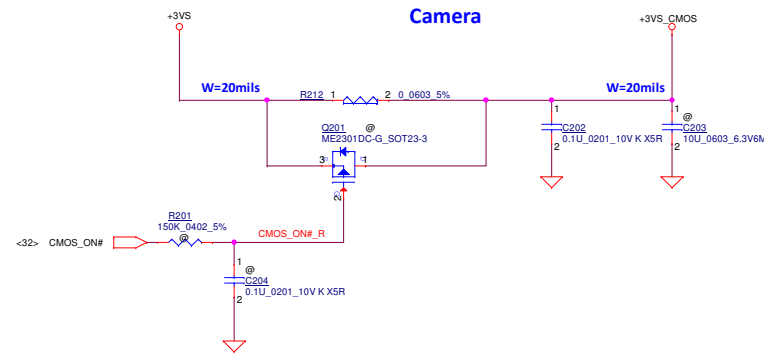
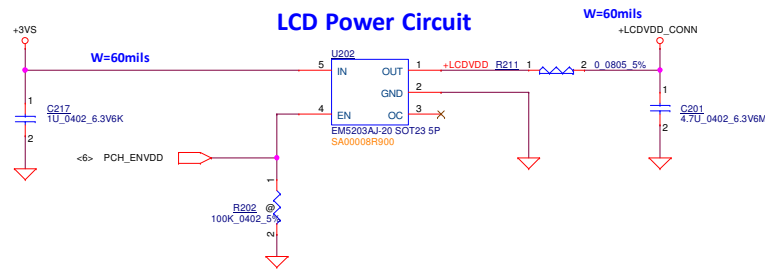


+3VS to +3VS_DGPU_AON



Memory Partition A

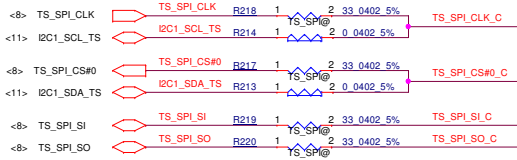


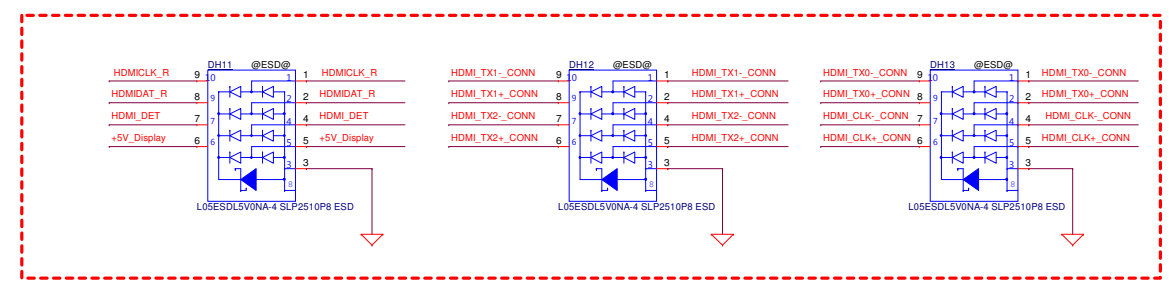
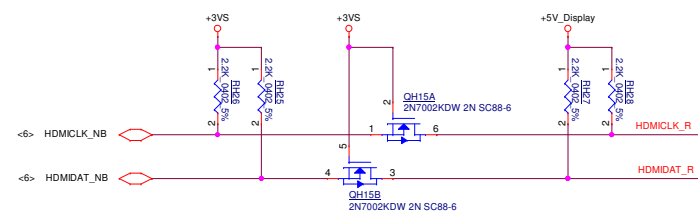
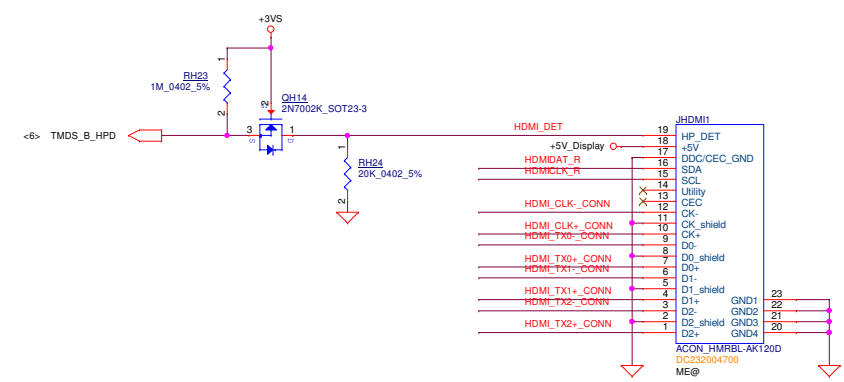
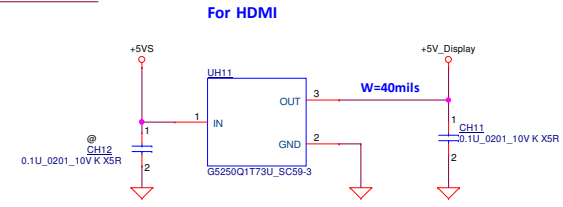
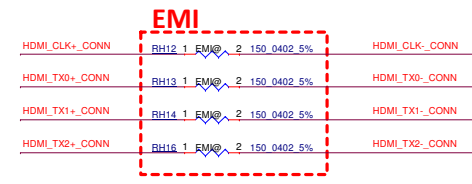
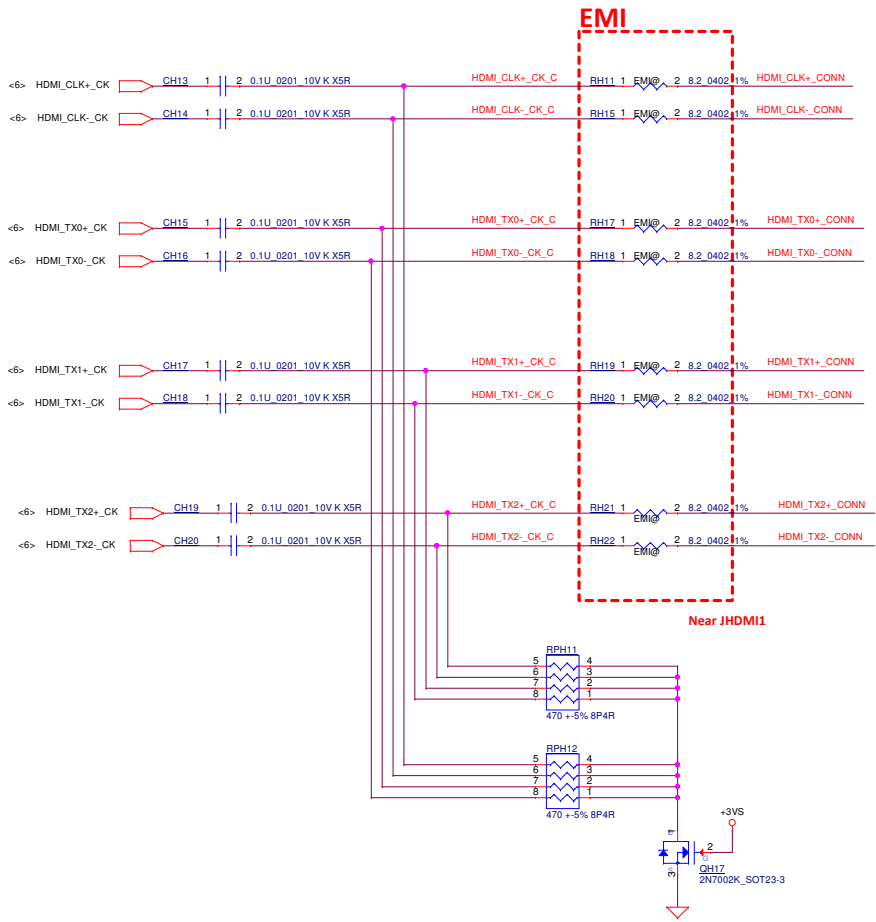


eDP CONN.

Elan Precise select by BOM (10 pins)		
1	PWR	PWR
2	CS	SCL
3	SCK	SDA
4	MOSI	Report switch
5	MISO	INT
6	Report switch	Reset
7	INT	Hsync
8	Reset	GND
9	Hsync	
10	GND	
Total	SPI (10 pins)	I2C (8 pins)

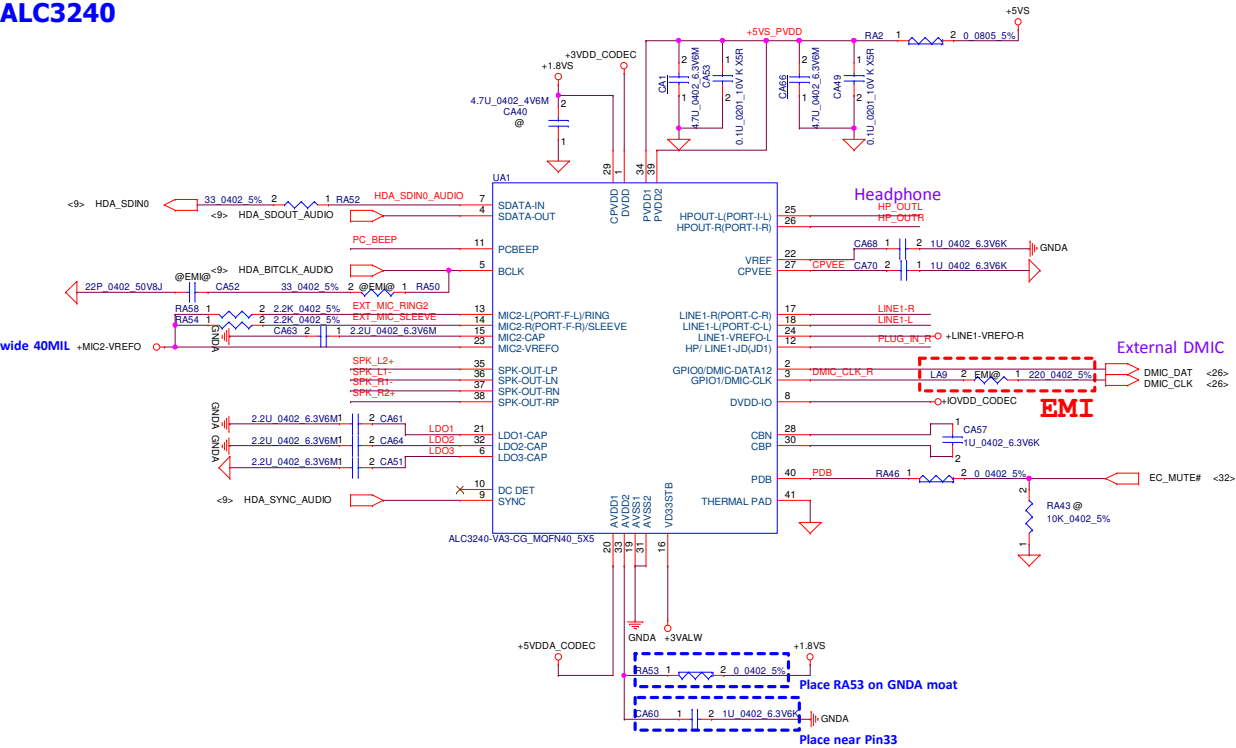
SPI & I2C PIN define	
1	PWR
2	SPI_Reset/I2C_Reset
3	Report_switch
4	GND
5	SPI_SCK/I2C_SCL
6	SPI_CS/I2C_SDA
7	SPI_MOSI
8	SPI_INT/I2C_INT
9	SPI_MISO
10	GND



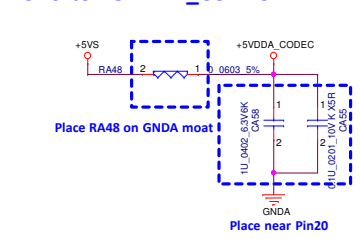


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Size		Document Number		Date: Wednesday, June 21, 2017		Sheet		27		of	
Custom		LA-E541P								Rev	
										2A	

ALC3240



+5VS to +5VDDA_CODECD



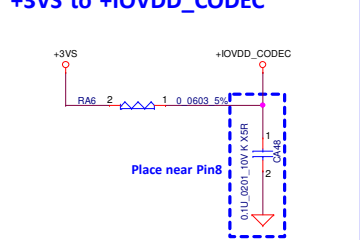
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
Intel Broadwell	1.5V (S0)	1.8V (S0)	3.3V (S0)	5V (S0)	3.3V (S0~S5)
Intel Skylake	V	V	V	V	V

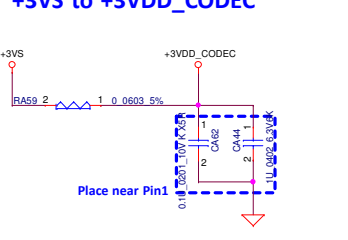
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

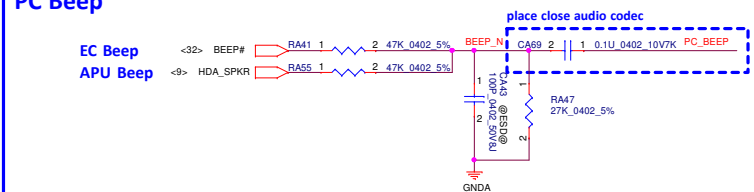
+3VS to +IOVDD_CODECD



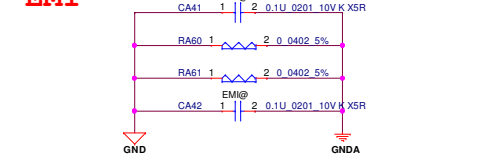
+3VS to +3VDD_CODECD



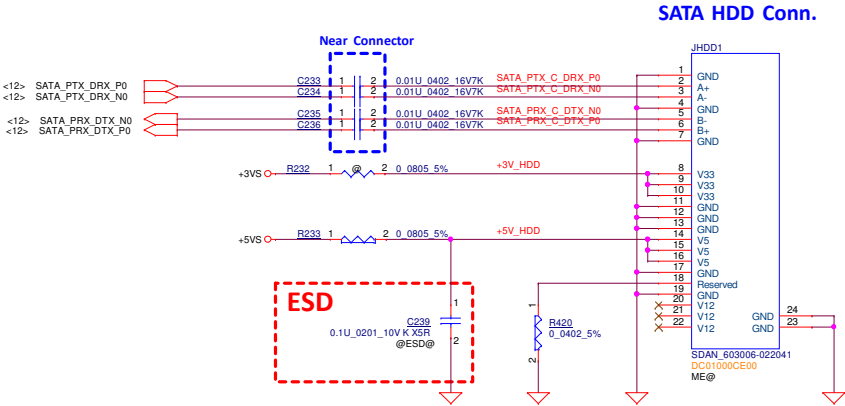
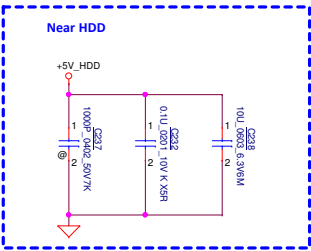
PC BEEP



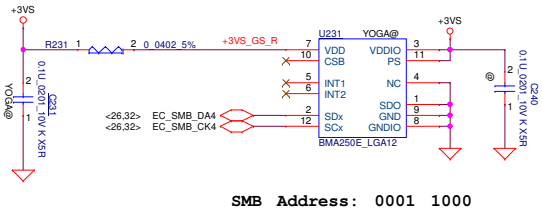
EMI



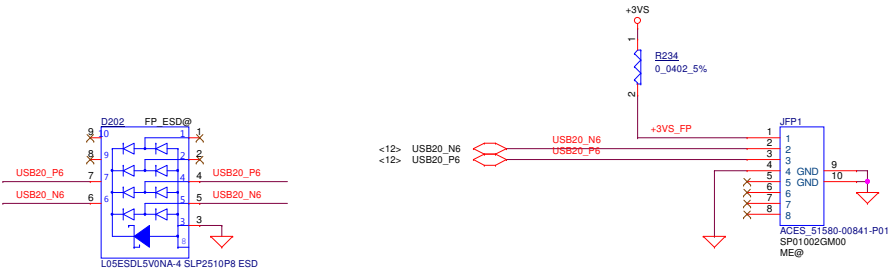
HDD



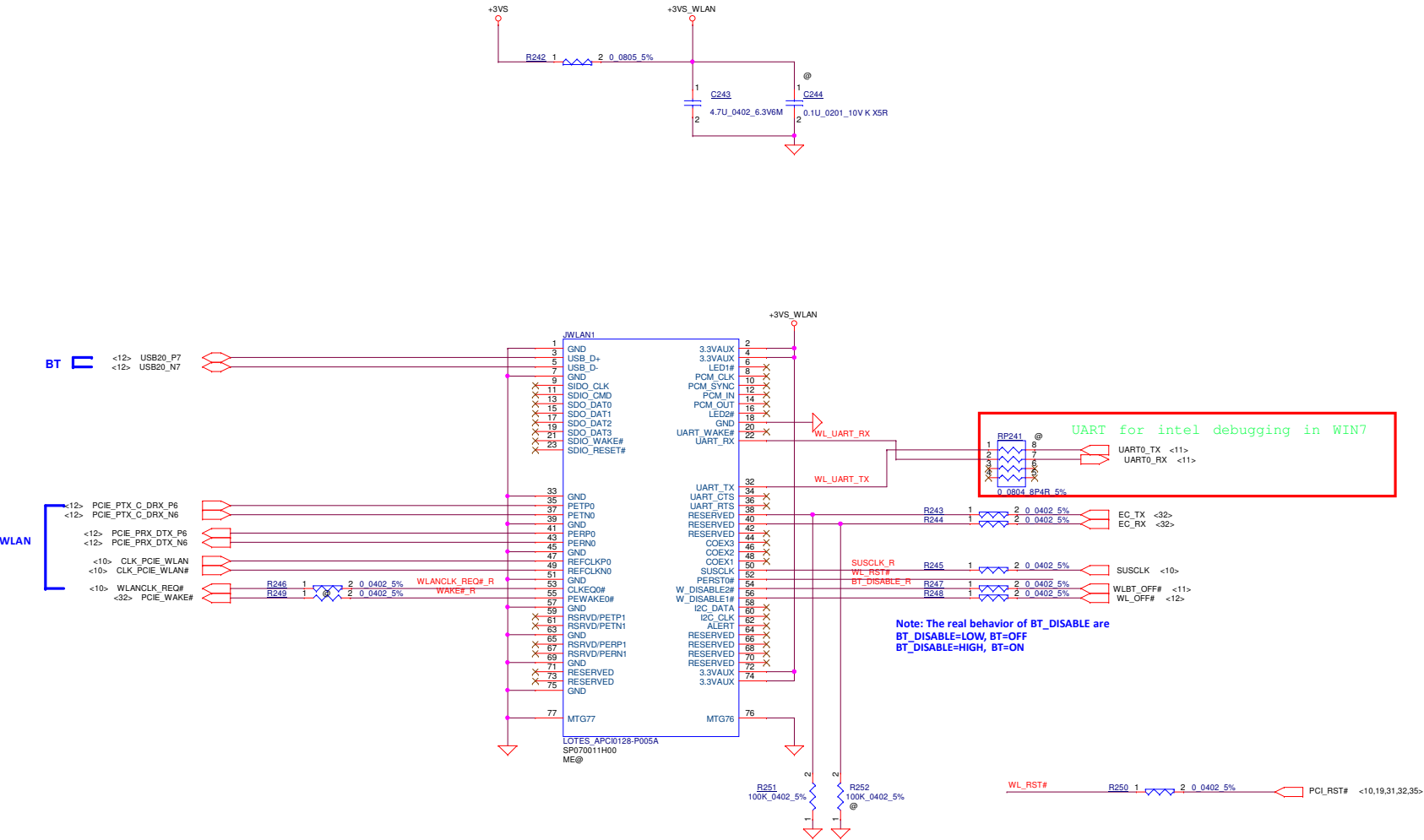
(G-Sensor for 360-degree reverse)



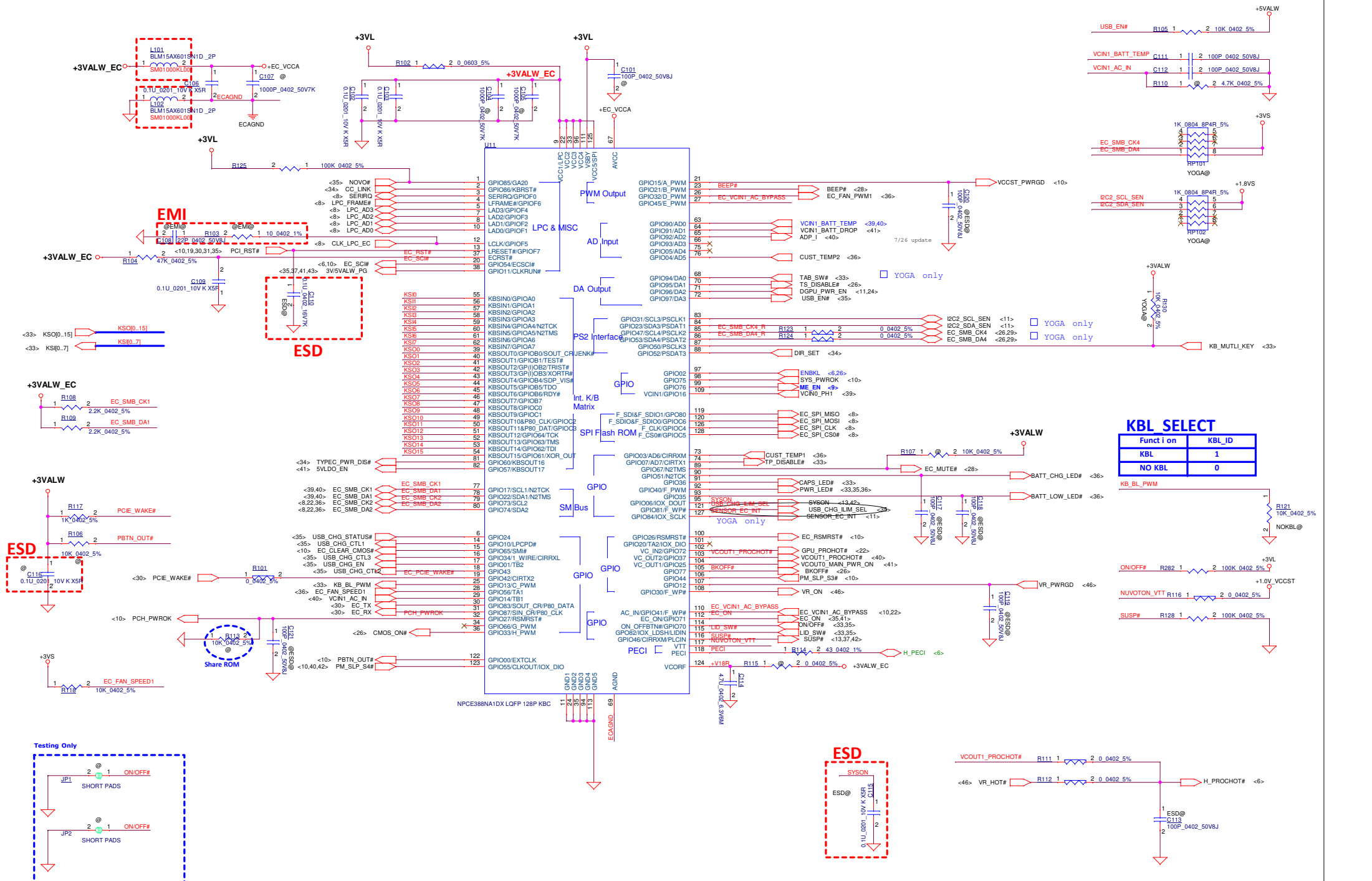
Finger Printer



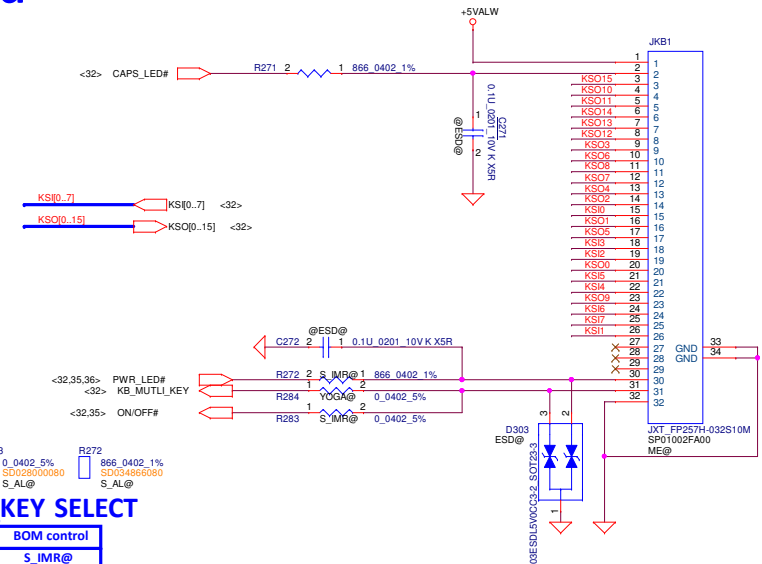
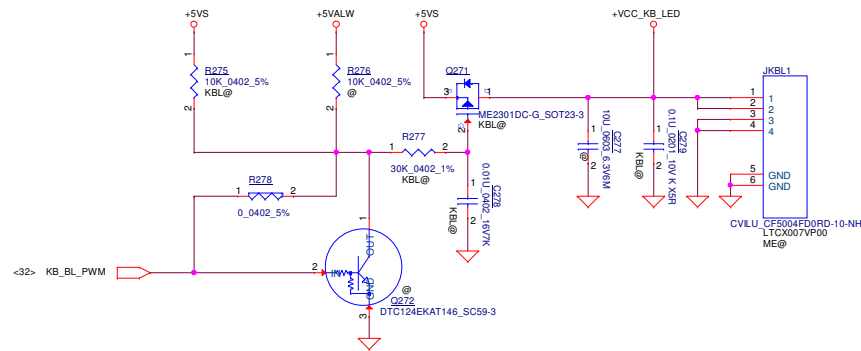
NGFF for WLAN / BT (E- KEY)



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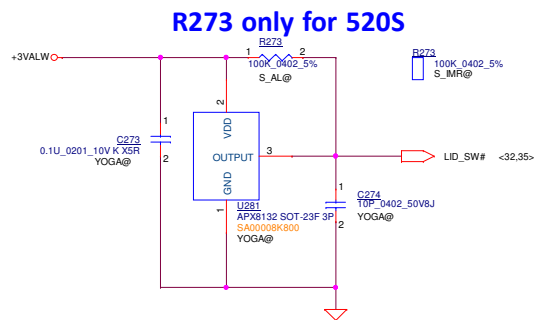
Keyboard



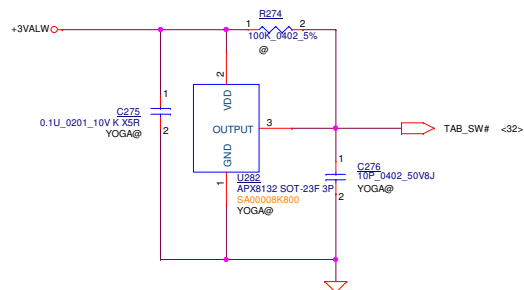
KB_MUTLI_KEY SELECT

Function	BOM control
Power Key (Cruze)	S_IMR@ S_AL@
Function Key (Alpine)	YOGA@

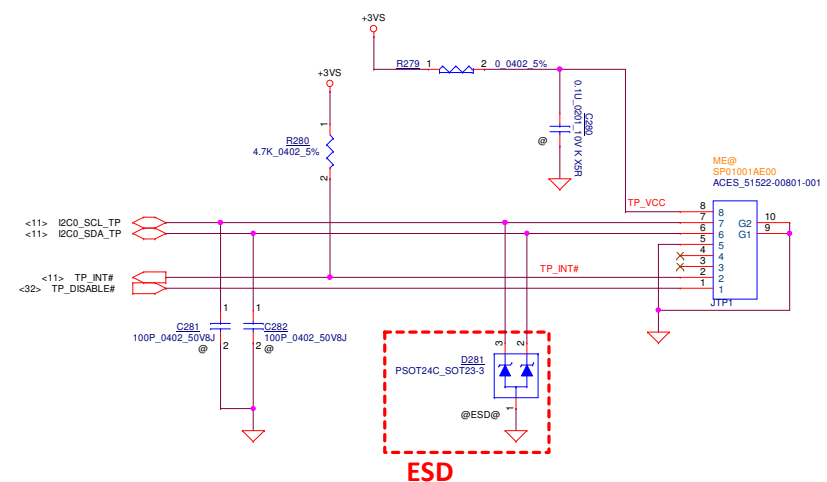
Hall -Sensor for 0-deg reverse (TOP)



Hall -Sensor for 360-deg reverse (BOT)

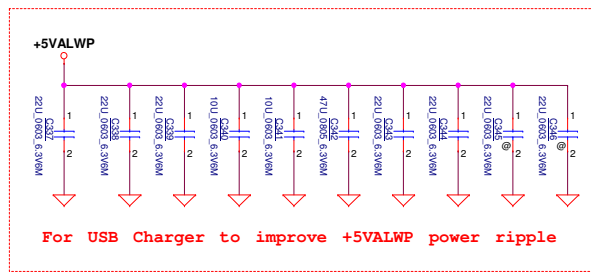


Touch Pad

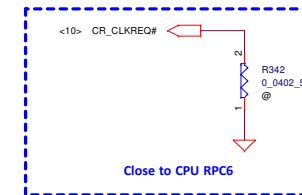
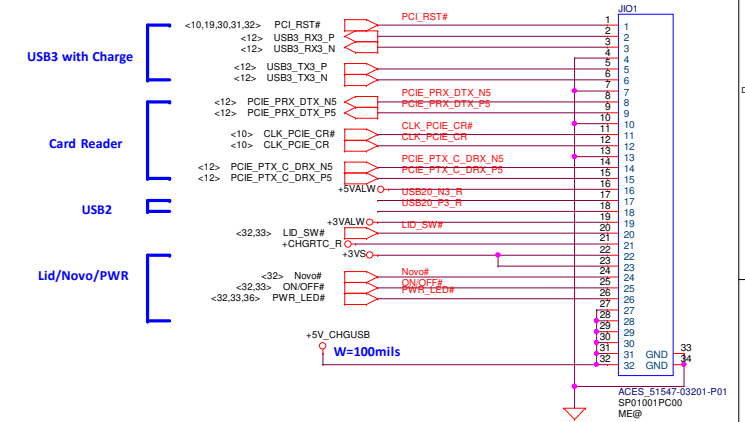


Security Classification		Compal Secret Data		Compal Electronics, Inc. KBL/KBD/Hall Sensor/TP	
Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title KBL/KBD/Hall Sensor/TP	Size Custom
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USB Charge

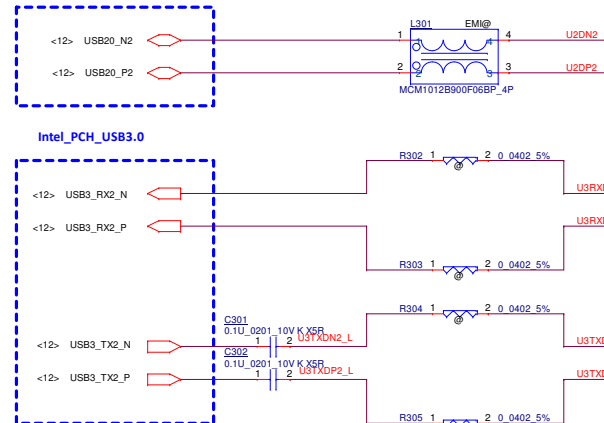
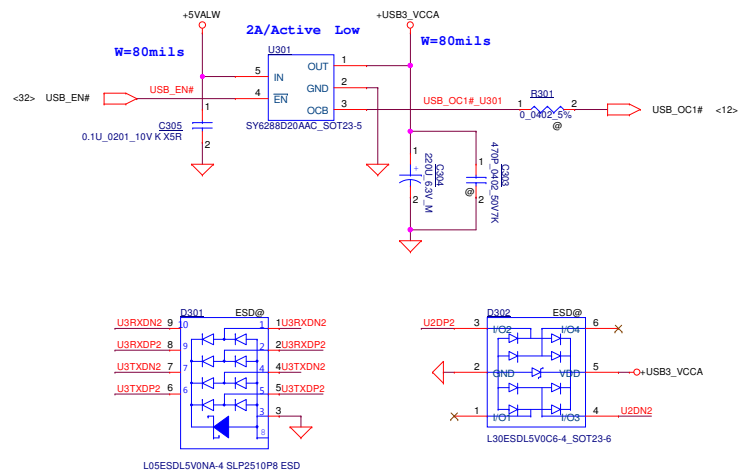


IO CONN

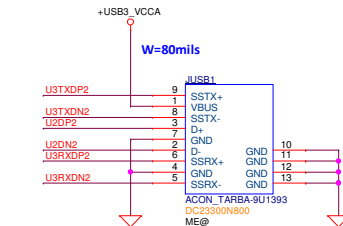


IO/B Function	Alpine	Cruze
USB3.0 w/charge	✓	
USB2.0 w/charge		✓
Card Reader	✓	✓
LID SW		✓
RTC	✓	✓
PWR PTN	✓	
NOVO BTN	✓	✓
PWR LED	✓	

USB3.0_Port

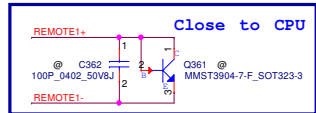
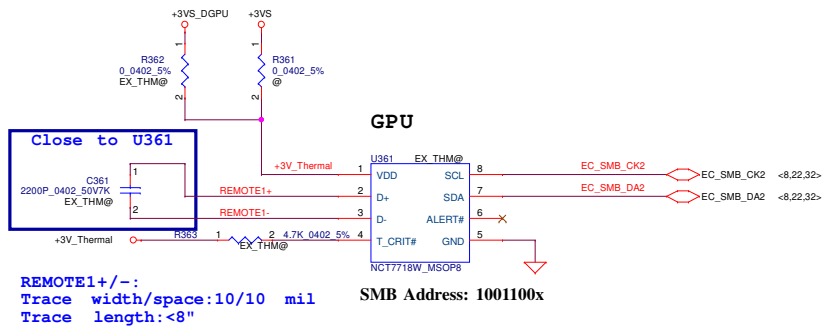


Place TX AC coupling Cap (C172,173). Close to connector

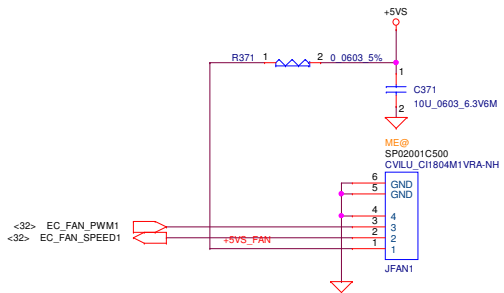


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				Size Custom	Document Number LA-E541P	
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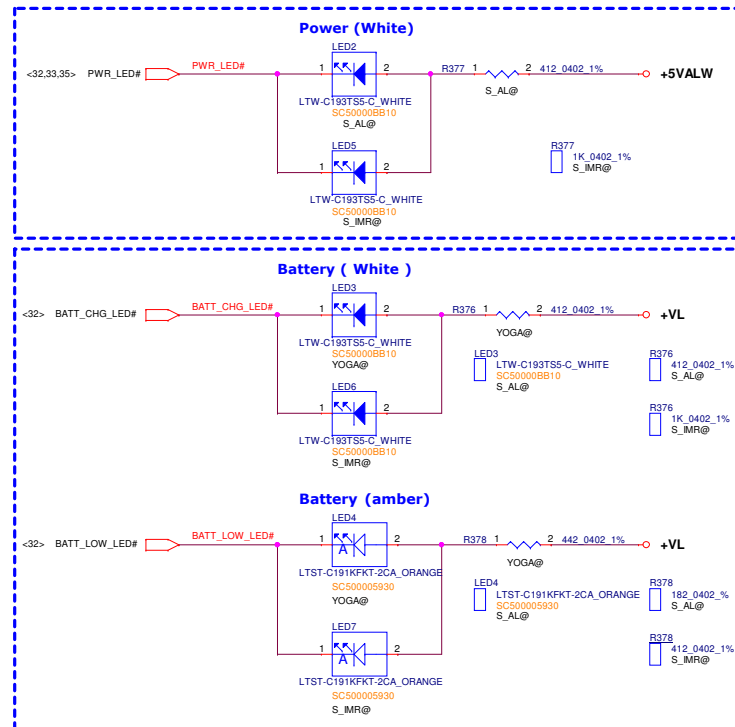
Thermal Sensor



FAN

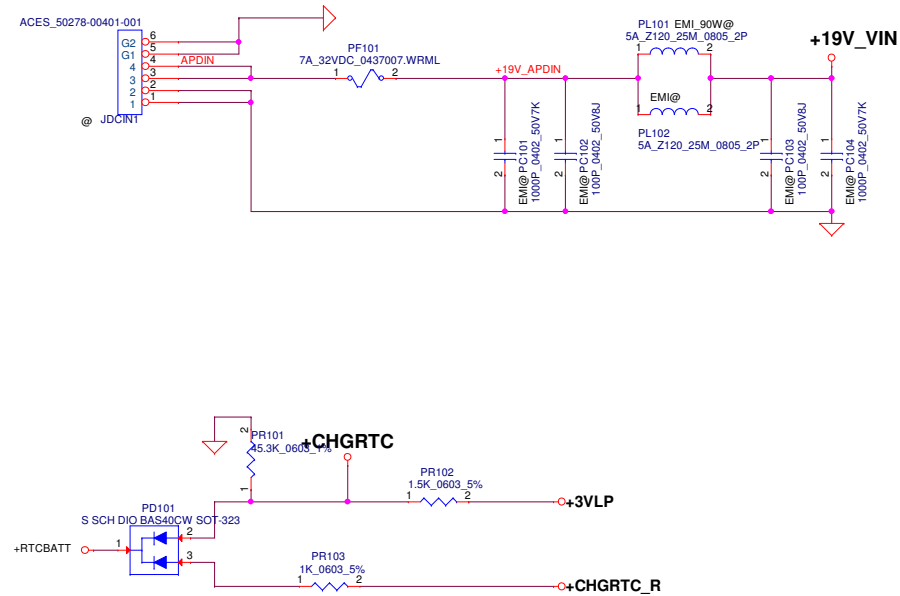


Power LED & Battery LED

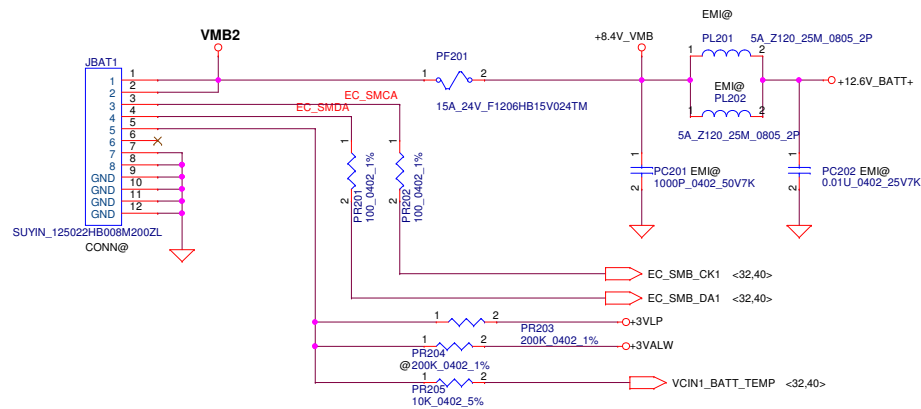


		Power (White) LED / Res.	Battery (White) LED / Res.	Battery (amber) LED / Res.
TOP	YOGA (YOGA@)	IO Board	R376 412 Ω	R378 442 Ω
TOP	S series (S_AL@)	R377 412 Ω	R376 412 Ω	R378 182 Ω
	S IMR (S_IMR@)	R377 1K Ω	R376 1K Ω	R378 412 Ω
BOT				

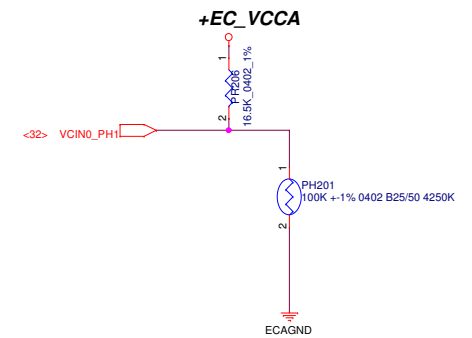
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	FAN / LED / Thermal Sensor
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				Document Number	
				KBL	
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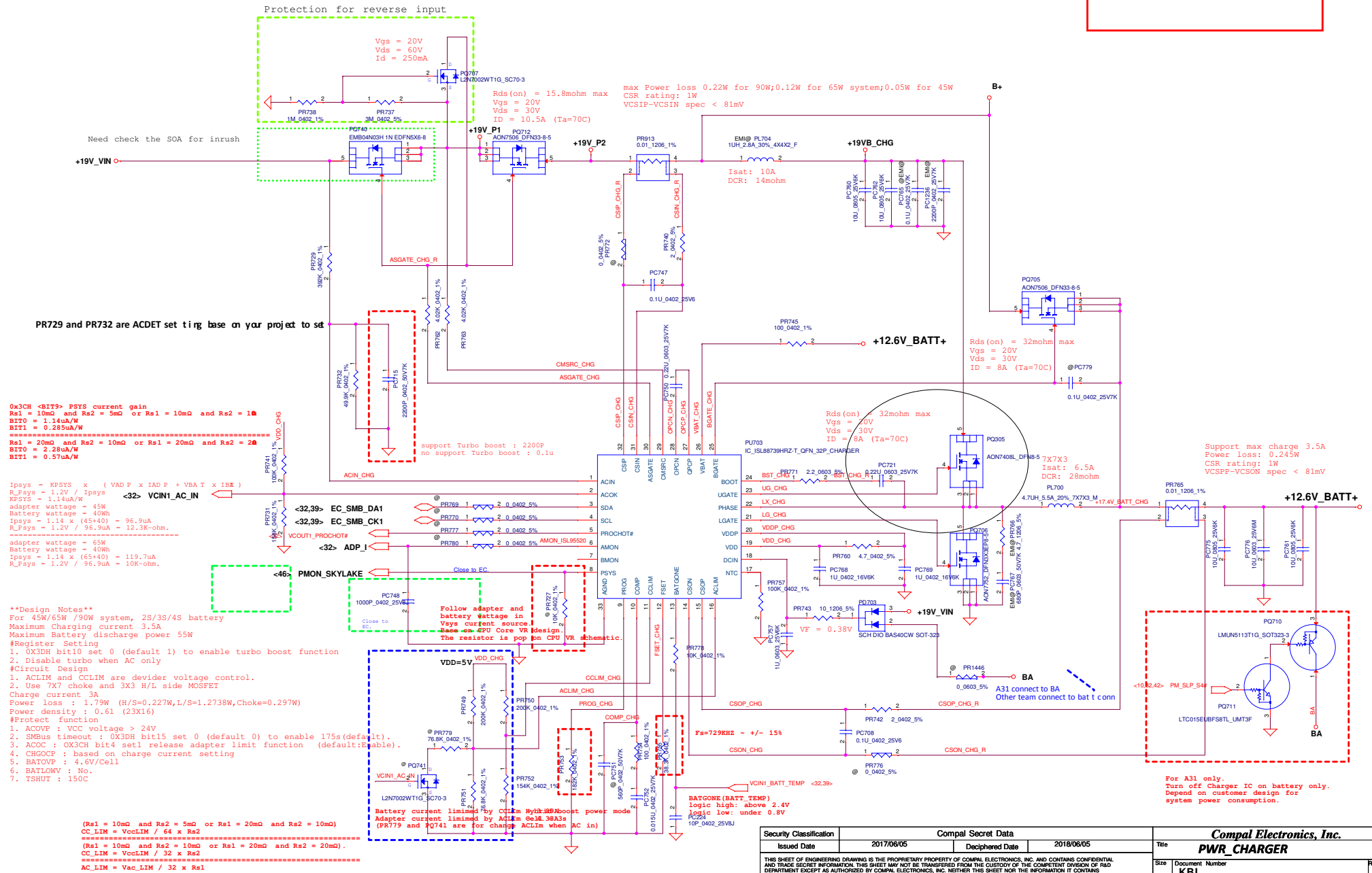


PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



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Module model information
ISL95520_Hybrid_Boost_V2.mdd



Module model information

SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd

Check pull up resistor of SP0K at HW side

keep short pad,
snubber is for EMI only.

Use 7x7x3 size when the layout space is enough.

Vout is 3.234V~3.366V

TDC=6A

Iocp=10A

<32,35> EC_ON

EN1 and EN2 don't be floating.
EN :H>0.8V ; L<0.4V

Fsw : 600K Hz

+3VALWP

+3VLP

Fsw : 600K Hz

EN1 and EN2 don't be floating.
EN :H>0.8V ; L<0.4V

2 Cell battery : Cin=10uF*2pcs
3 Cell ~ 4 Cell battery : Cin=10uF*1pcs

keep short pad,
snubber is for EMI only.

Vout is 4.998V~5.202V

TDC=6A

Iocp=10A

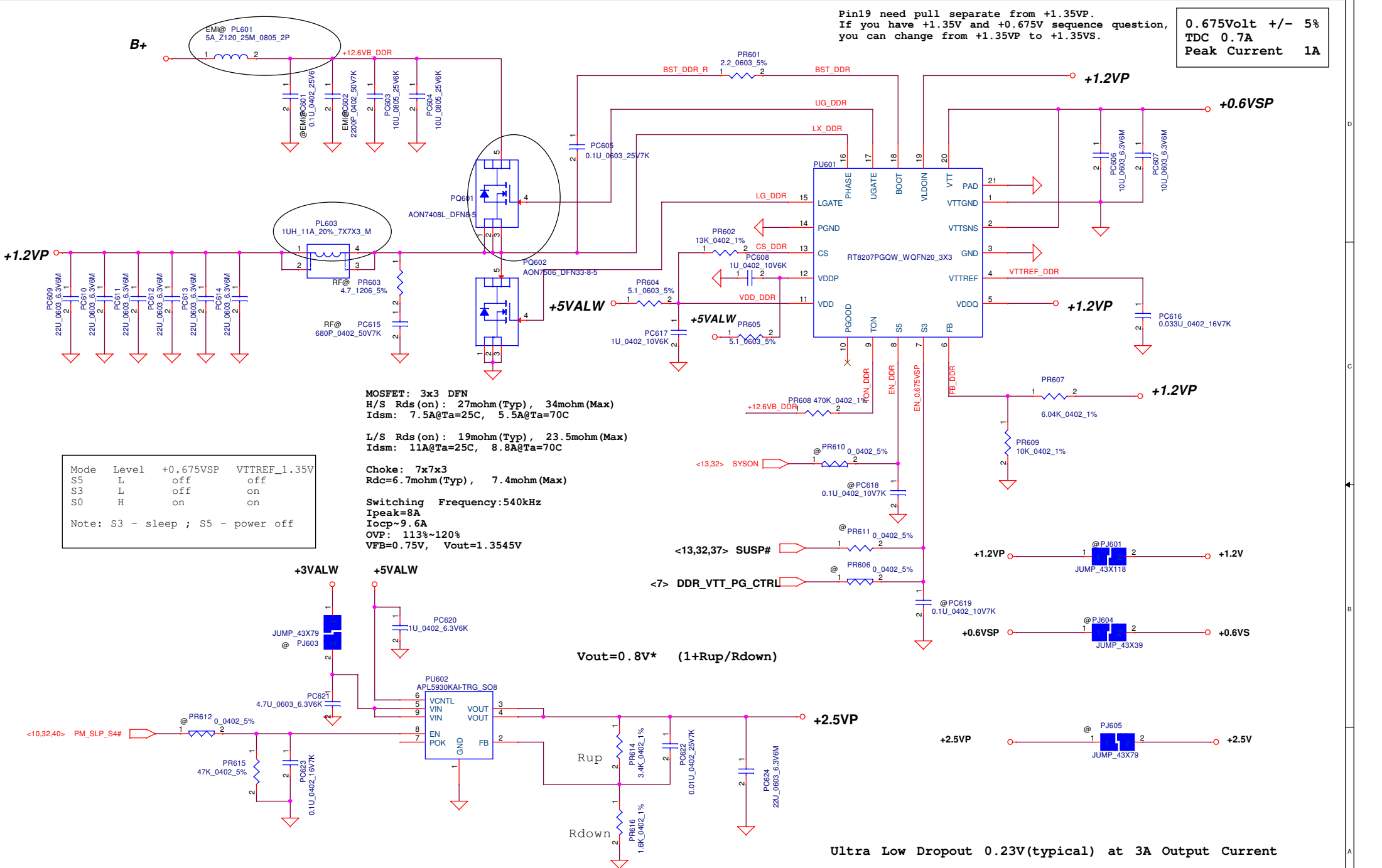
+5VALWP

+5VLP

+19VB_5V

VCIN1_BATT_DROP <32>

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Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

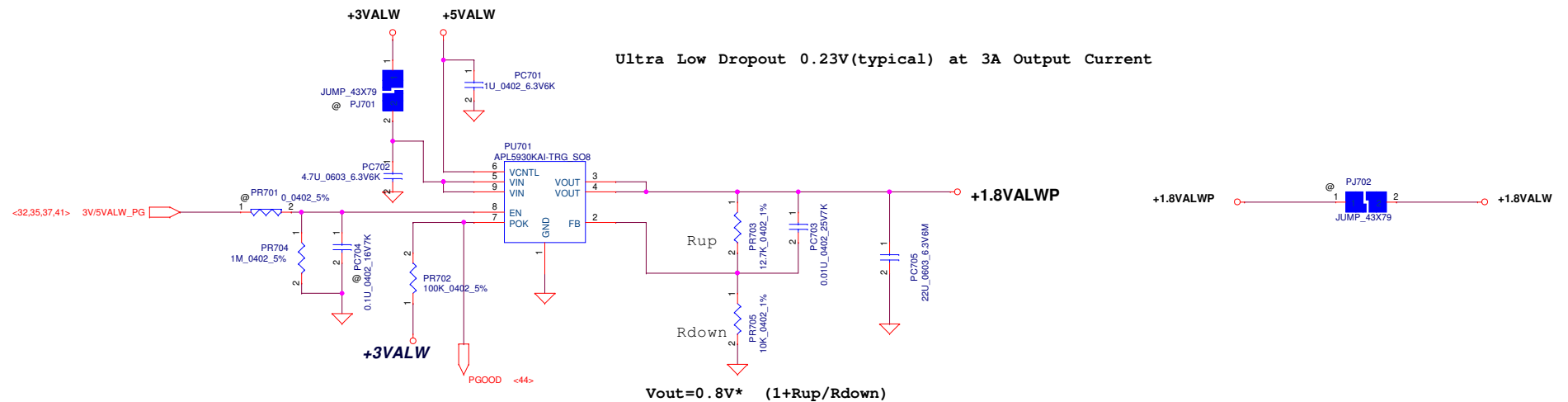
Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency: 540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

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Size	Document Number	Rev		2A	
Custom	KBL	Date:		Wednesday, June 21, 2017	
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Module model information

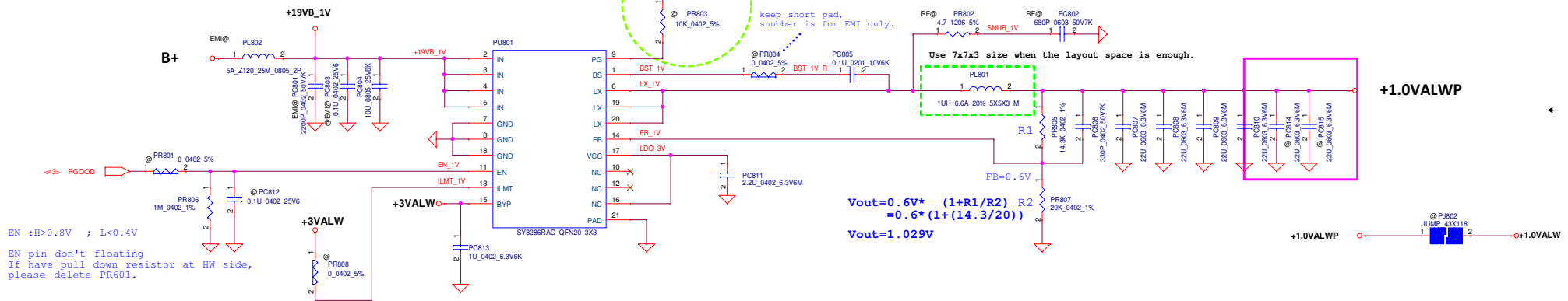
APL5930_V2.mdd



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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	APL5930
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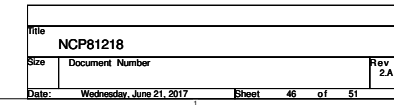
Module model information

SY8286_V1_single.mdd
SY8286_V1_dual.mdd

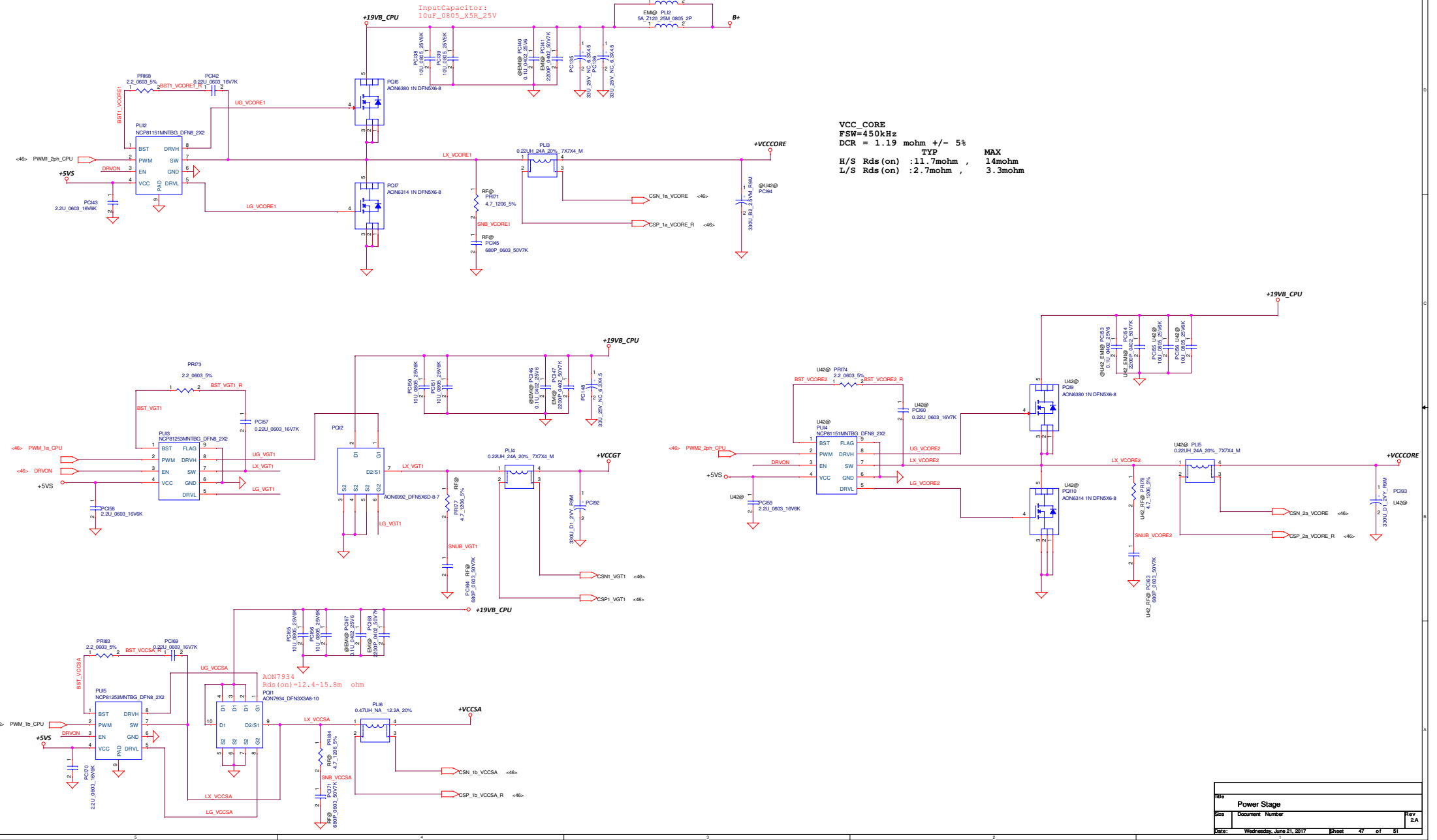


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Issued Date	2017/06/05	Deciphered Date	2018/06/05	Title	SY8286
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A



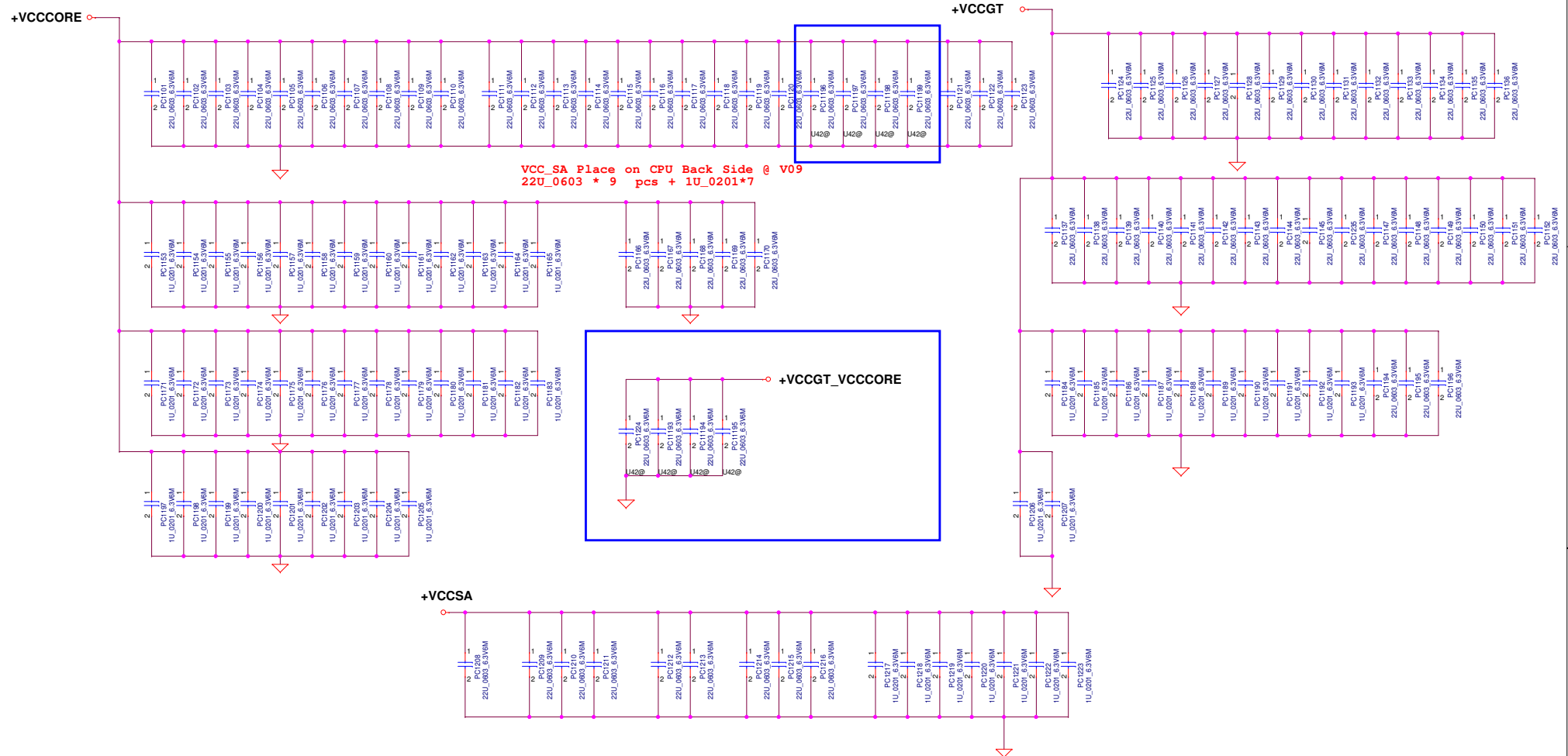
CPU POWER STAGES



Title			Power Stage
Doc	Document Number	Rev 2.A	
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VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 36pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 32 pcs +1U_0201*12 pcs



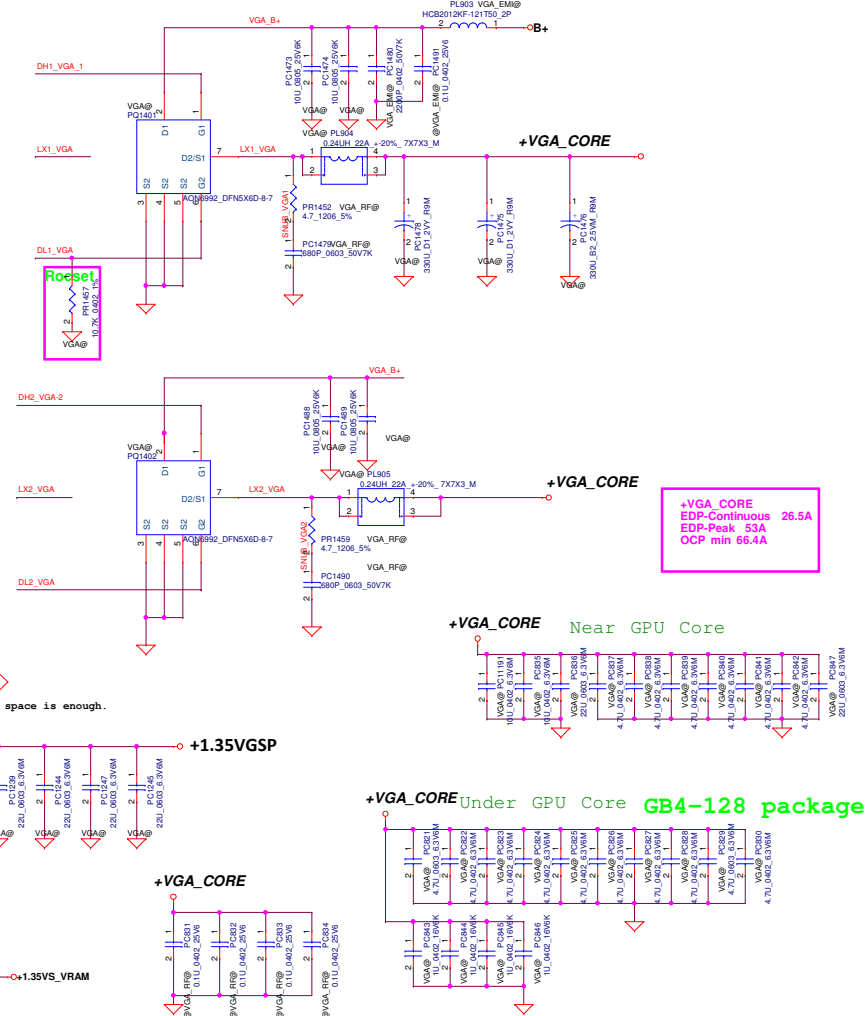
PWM-Vid Spec	Config A	Config B	Config C
Vmin	0.6V	0.6V	0.65V
Vmax	1.2V	1.2V	1.15V
Vboot	0.875V	0.9V	0.9V
Voltage step	6.25mV	6.25mV	25mV
N of Voltage steps	96	96	20
PrR8	39K	20K	39K
PrR7	39K	20K	30K
PrR10	1.5K	2K	3K
PrR20	30K	19K	24K
PrR21	1.5K	0	3K
C	1.5nF	2.7nF	1.8nF

```

Rl=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rl/(Rref1+Rl)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

```

VGA® PR1468 Pull high on HW side
1K 0402 5%



+VGA CORE
EDP-Continuous 26.5A
EDP-Peak 53A
OCP min 66.4A

+VGA_CORE Under GPU Core **GB4-128 package**

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

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Issued Date	2017/06/05	Deciphered Date	2018/06/05	PWR-CPU _GFX		Rev 2A	
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